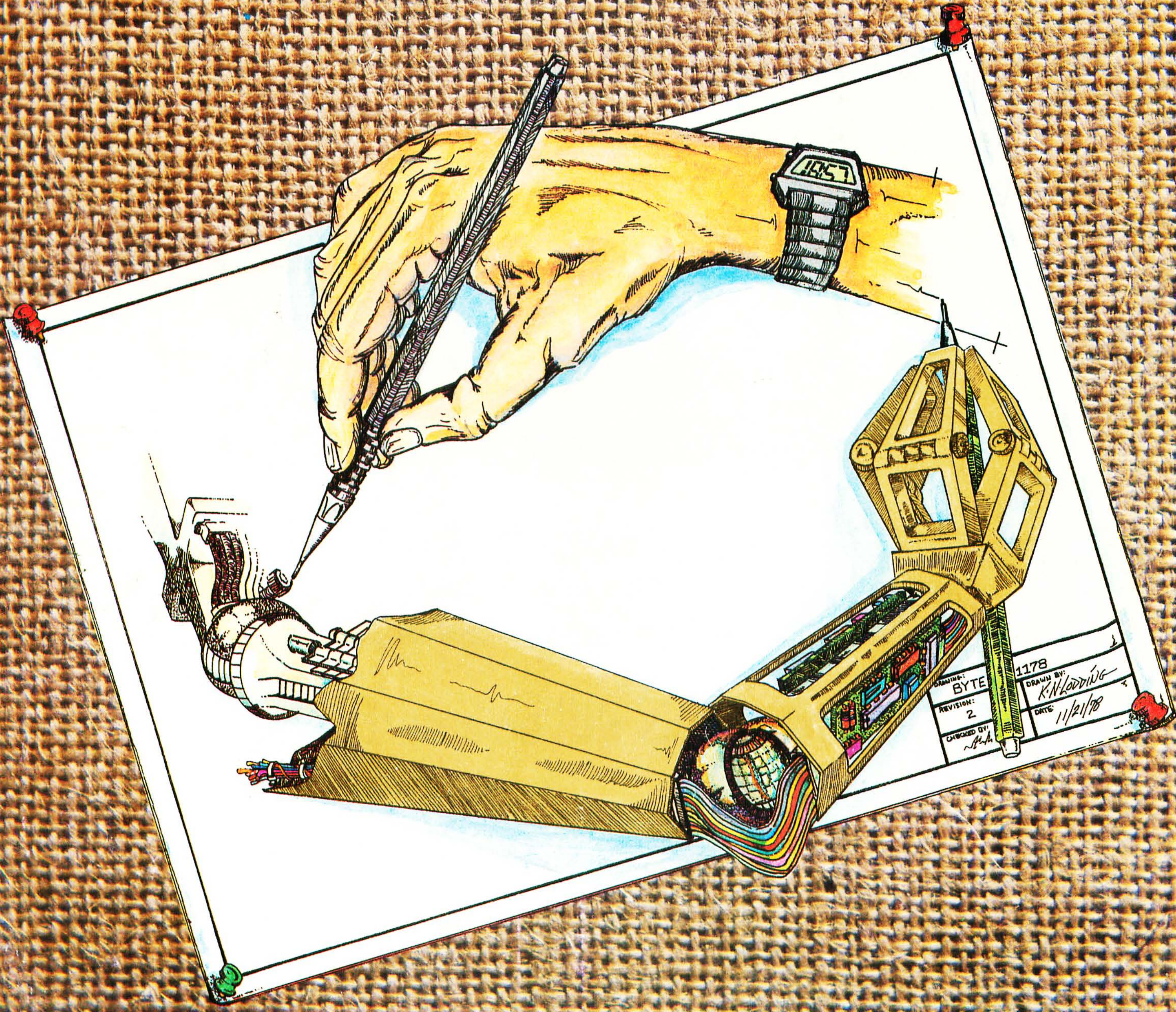
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BYTE

the small systems journal







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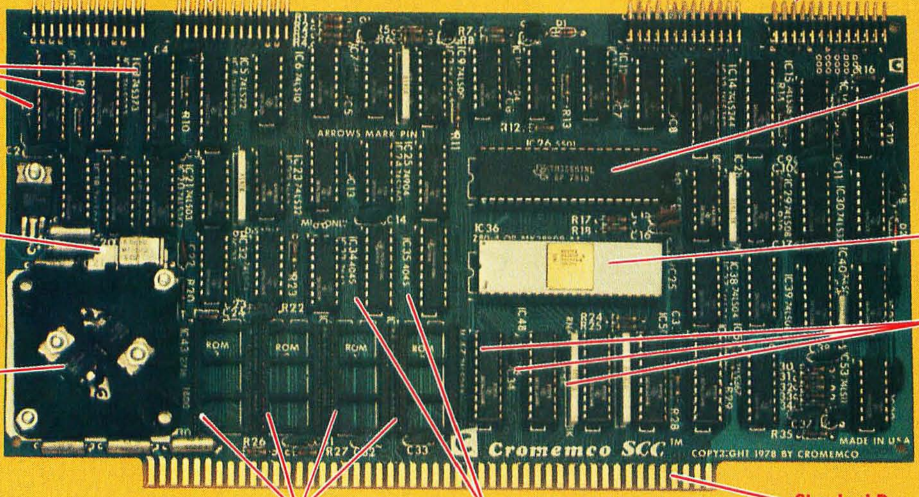
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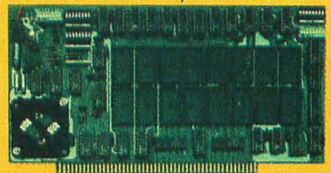
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BYTE February 1979
Volume 4, Number 2

Foreground

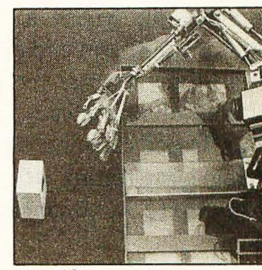
Background

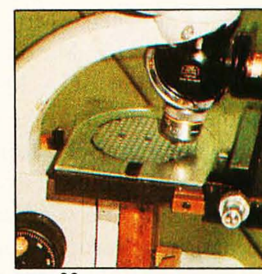
Nucleus

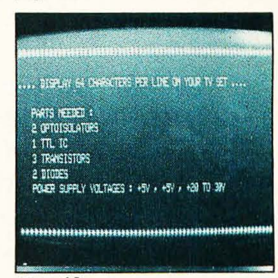
Cover Art: CLOSING THE LOOP, *by Ken Lodding, after M C Escher.*

AUDITED PAID CIRCULATION ABC

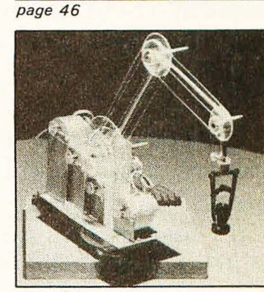

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page 84

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In this BYTE

This month's cover, "Closing the Loop," by Ken Lodding, is our version of the famous original, "Drawing Hands," by the Dutch artist Maurits Cornelis Escher (1898-1969). Much of Escher's work deals with mathematical subjects, and the idea of a robot hand drawing a human hand (and vice versa) seems particularly appropriate to this month's theme of robotics.

In **Designing a Robot from Nature,** Andrew Filo begins a 2 part series about a robot arm and eye mechanism designed to simulate certain biological features of amphibians. Study of the frog's insect catching capability leads to some interesting design shortcuts. Read **Part 1: Biological Considerations.** *page 12*

6809 designers Terry Ritter and Joel Boney of Motorola continue their discussion of **A Microprocessor for the Revolution: The 6809** in **Part 2: Instruction Set Dead Ends, Old Trails and Apologies.** This lively question and answer section reveals the design philosophy that went into the 6809, the successor to the Motorola 6800 processor. *page 32*

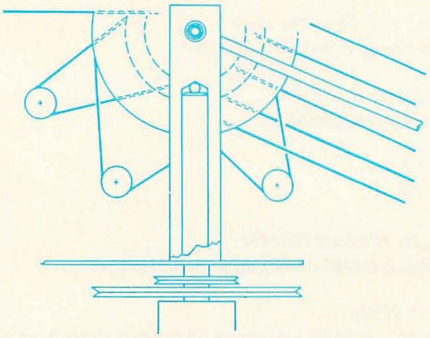
If you have just bought a Radio Shack TRS-80 or a similar microcomputer, you may have asked "How can I use a standard television receiver as a video display unit?" Timothy Loos answers the question with high resolution results in his article **Use Your Television Set as a Video Monitor.** *page 46*

In **Another Plotter to Toy With,** Peter A Lucas describes a novel approach to building a homebrew plotter using an Etch-A-Sketch® unit, which is available in toy stores. *page 66*

Punched cards are still very much with us. For experimenters who want to make use of this venerable storage medium, Anthony Schaeffer describes a homebrew card reader in **The Eclectic Card Reader.** *page 70*

The Lear Siegler ADM-3A "dumb" terminal can provide terminal oriented systems with this essential component in a reasonably priced kit. Paul Franson describes his experiences while **Assembling the ADM-3A** from a kit. *page 76*

The development of a hobbyist robot arm capable of being controlled by a computer will open up a new area of control applications. The robot arms available on this level today are fairly small and weak. Keith Baxter and Timothy Daly describe their design for **A Hobbyist Robot Arm.** *page 84*



The stepping motor is an attractive device for personal computer applications because of its versatility and price. Paul Giacomo begins a 2 part **Stepping Motor Primer** in this issue. **Part 1: Theory of Operation,** gives the background on the device. The second part, in next month's BYTE, will cover interfacing to a computer. *page 90*

We recently presented a Fast Fourier Transform program (December 1978 BYTE) written in BASIC. (FFTs are used to analyze periodic signals such as music and speech for frequency content.) This month, Dick Lord's **Fast Fourier for the 6800** describes a 6800 assembly language version that is approximately ten times faster than the BASIC version. *page 108*

Many personal computer owners use their systems to develop game programs, one of the most exciting and creative applications of this technology. There are probably as many ways to go about developing game programs as there are people implementing them. H L Stuck is one such implementer and he has several ideas about **Approaching Game Program Design** presented in his article in this issue. *page 120*

If your computer is currently running a programming language that allows only integer manipulation, do not despair. You can still have a lot of fun exploring real numbers. Jef Raskin describes how to perform **Unlimited Precision Division** using only an integer BASIC package. *page 154*

Part 2 of **Build a Computer Controlled Security System for Your Home** by Steve Ciarcia concentrates on software. With a bit of effort readers can implement this sophisticated system, which uses infrared beams and ultrasonics (among other techniques) to keep their homes secure. The 3 part series concludes next month. *page 162*

It can be very disconcerting to have an error appear in a long string of information being loaded from a tape. Usually this means that the entire operation must be started over again. Michael Wimble describes the **Hamming Error Correcting Code** to help reduce this problem. *page 180*

With the advent of inexpensive mass storage devices such as the floppy disk, the use of files is becoming more widespread in personal computing. Mark Klein begins a 2 part discussion of what files are and how to use them in **Files on Parade, Part 1: Types of Files.** *page 186*


"My Shugart
followed me home."

Editorial

The Current State of Robotics

by Carl Helmers

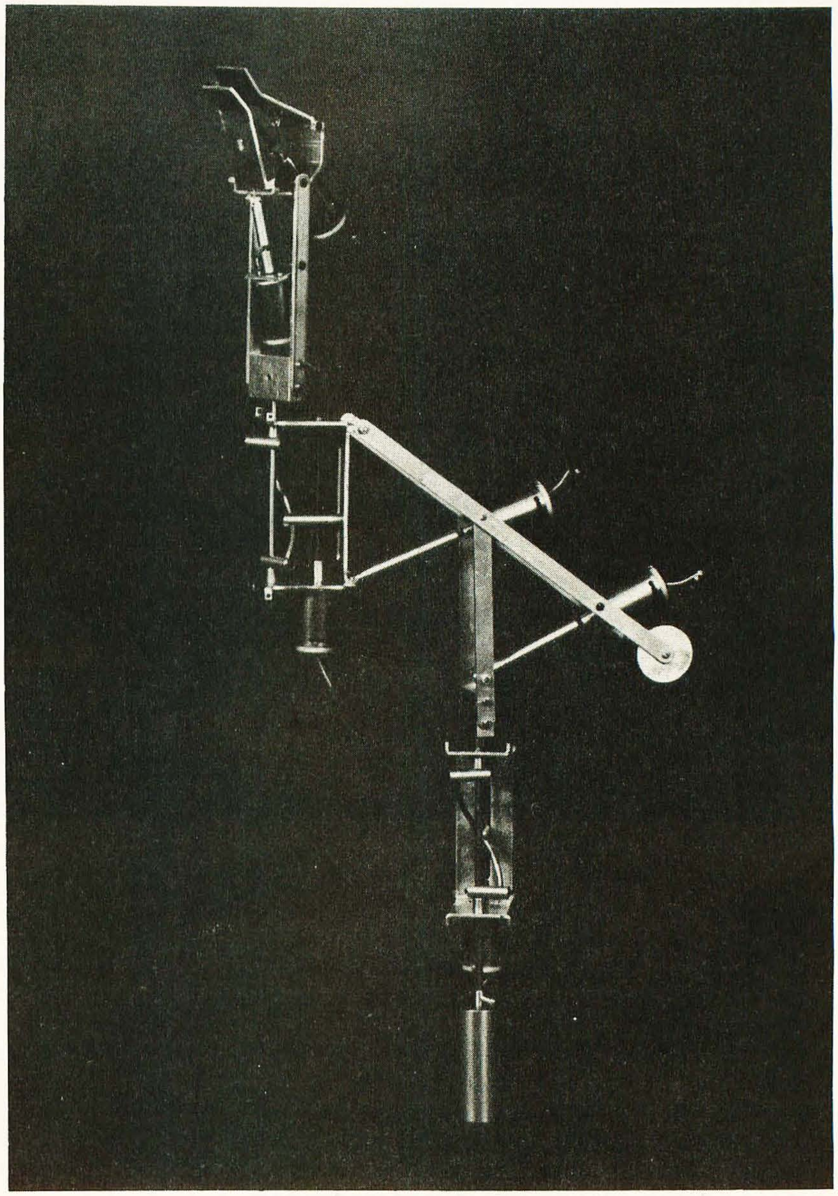


Photo 1: Robot arm, which was assembled by yours truly, using a kit of parts supplied by Gallaher Research Inc for $400. It was purchased in September 1978 and was assembled in about two hours from the parts supplied. It has no sensors, and no attention to that minor detail of how to drive the 6 V 4 A (8 A peak) loads of each motor. Since this item was purchased, Mr Gallaher informs us it has been withdrawn from the market.

Exciting developments are on the horizon of the field of automated intelligent mechanisms. With its cover theme of "the arms race" this issue of BYTE reflects the trend towards perfection of an inexpensive robot arm that is within the construction capabilities of the computerist. A number of individuals are experimenting with a mechanism controlled by a small computer. At present the efforts *are* but experiments—with no obvious application as products for living. But out of this spirit of experimentation new fields of endeavor grow.

Robotics is not yet a consumer products field, unless one would include the entertainment automatons (found at amusement parks), which are controlled by minicomputers of an older computer technology. Of course, robotic techniques are already in commercial use, as with intelligent automated machines operating in manufacturing and commercial office environments. I know of contemporary uses of robotic arms in the commercial manufacturing of automobiles and jet engine turbines. There is also a well-known robot mail cart which delivers inter-office mail in large buildings in many cities. It can not yet negotiate elevators, so it is confined to one floor at a time and thus is most cost efficient in flat buildings.

The Stanford Research Institute robot called Shakey, which is described in Bertram

Continued on page 194

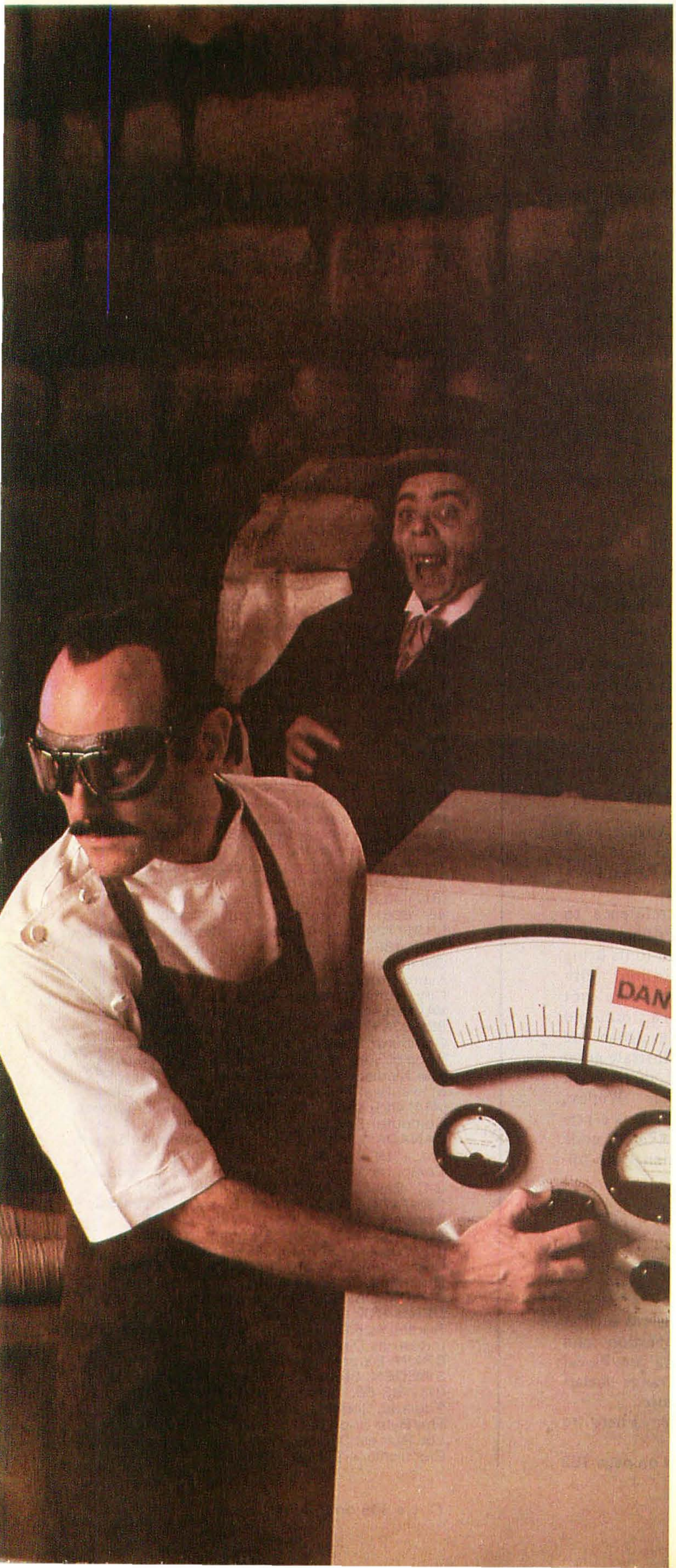
Photo 2: Of course, there are marionettes. This little beastie cost us $32.50 including tax at a store called Geppetto's located in a pushcart at Boston's Faneuil Hall marketplace. It is a fully assembled mechanical system, but it lacks the DC motor actuators necessary to pull strings.



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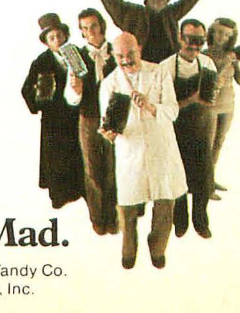
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Letters

ABACUS ANSWERS

The answers to William B Adams' abacus query (November 1978 BYTE, page 145) can be found in *Number Words and Number Symbols* by Karl Menninger, the MIT Press (1970).

The Roman abacus had four counters below the bar and one above. The Japanese *soroban* has five counters below and one above. The Chinese *suan pan* has five counters below and two above. The Russian *schyot* has ten counters and no bar, with the two middle counters colored differently from the rest (the counters run horizontally instead of vertically). The three latter forms are widely used, even today, side by side with electronic digital calculators.

Menninger's fascinating and scholarly book devotes about 90 pages to the history of the abacus and counting boards.

Richard D Geckler
135 Belday Rd
Pasadena CA 91105

MORE ON THE ABACUS

A letter from William B Adams in November 1978 BYTE, page 145, questioned the designation of the abacus pictured in the interesting article on "A Short History of Computing" by Keith S Reid-Green that appeared in July 1978 BYTE, page 84. Perhaps I can help answer Mr Adam's question.

First, Mr Reid-Green is correct. The abacus pictured in his article is a traditional Chinese abacus having two upper (or *heaven*) beads and five lower (or *earth*) beads. Mr Adams says his machine has two upper and five lower beads but "is clearly marked 'Japan' and *soroban* in small print. . . ." No problem; early Japanese sorobans (Japanese for abacus) used the Chinese bead configuration. Eventually the number of upper beads was reduced to one and in 1891 Garyu Irie reduced the number of lower beads to four.

The modern Japanese configuration is more efficient than the traditional Chinese abacus, assuming the user has memorized a number of fingering rules. For example, in 1946 an employee of the Japanese Postal Administration defeated a representative of the US occupation force in a contest that matched a soroban against an electric calculator. The abacus won in addition and subtraction (50 problems of 3 to 6 digits), division (6 to 12 digits per problem) and composite problems. Only in multiplication did the calculator win.

Incidentally, Mr Reid-Green implies that "Roman and European traders" learned the principle of the abacus from the Chinese. Actually the Romans had developed a kind of abacus before the time of Christ. The present Chinese abacus was first mentioned in a book from the Yuan Dynasty of the 14th century. The Chinese call their abacus *suan-pan*, while *abacus* is of uncertain origin.

For a quick introduction to the abacus, Mr Adams might wish to refer to chapter 2 of *Number Machines*, a short book on the abacus, slide rule and calculator I have written (David McKay Company, 1977).

Forrest M Mims III
Contributing Editor, *Popular Electronics*
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San Marcos TX 78666

RATFOR RATIONAL

I enjoyed your special August 1978 BYTE issue on Pascal. I shall be looking forward to more software in Pascal from readers of BYTE (hint, hint).

I did note a passing reference to RATFOR in your cover writeup and I would like to take exception to its being classified (even by implication) with FORTRAN. For those who are not familiar with RATFOR, it is a structured language created by B W Kernighan and P J Plauger as a vehicle to illustrate good programming practices in their book *Software Tools* (Addison Wesley, Reading MA, 1976). RATFOR is a preprocessor which converts RATFOR code into FORTRAN. It implements the following structures:

IF . . THEN . . ELSE
WHILE
REPEAT . . UNTIL
FOR (iterative)

as well as some useful extensions such as file inclusion, string declaration and token replacement. Lacking are Pascal features such as recursion, range declarations and the case of structure.

At the University of Malaya here we

Continued on page 152



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Designing a Robot from Nature

Part 1: Biological Considerations

Andrew Filo
4621 Granger Rd
Akron OH 44313

Note:
This article contains highly stylized biological drawings, not to be understood as accurate histological representations.

One of the major problems involved in producing a robot is the design of a sophisticated "brain" and "nervous system" for the robot. Since World War II there has been an ever intensifying research effort to produce just such an artificial intelligence.

Presently, there are two distinct groups performing this research: neural cybernetists and cognitionists. The first group, the neural cybernetists, are concerned with studying the nervous systems and brains of living organisms in hopes of emulating them with machinery. To date, this type of research has provided much information about neurons and the entire nervous system in general. From this research, neural cybernetists have developed noncomputer *perceptrons* (artificial intelligence machines). Notable among the perceptrons already built is a system modeled after the pigeon's nervous system, used in missile navigation. The cognitionists believe, however, that highly evolved computer software is the best way to produce artificial intelligence. Examples of the work in this area are articles by Michael Wimble and Ralph Hollis ("Artificial Intelligence, An Evolutionary Idea, Parts 1 and 2," May and June 1977 BYTE, pages 26 and 100; and "Newt: A Mobile, Cognitive Robot," June 1977 BYTE, page 30).

Although the neural cybernetists and cognitionists are essentially striving toward the same goal, they often refuse to recognize each other's research effort. Two books that exemplify the conflict in views are *The Computer and Thought*, edited by E Feigenbaum and J Feldman, and *The Search For Robots*, by A J Cote Jr (see bibliography at end of part 2 next month). In the latter, Cote describes the work of neural cybernetists in artificial intelligence and robot research.

Cote argues that the computer is a poor device for use in constructing an artificial intelligence. He supports his claim with the old misconception that computers are electronic brains. He feels that cognitionists have convinced themselves that a computer can become intelligent if programmed properly. Conversely, Feigenbaum and Feldman's book, a collection of published papers, has an opening chapter that, among other things, explains why the editors have excluded all neural cybernetics papers. In part, they argue, cognitionists "believe that intelligent performance by a machine is an end difficult enough to achieve without starting from scratch," as a neural cybernetist would have to. It is unfortunate that these two groups continue to hold these views even though the books were written more than a decade ago, since, in my view, combining the two philosophies is the only practical way for researchers to understand and develop a truly sophisticated artificial intelligence.

My interests in this field prompted me to try to fill the void created by cognitionists and neural cybernetists by developing my own philosophy pertaining to the study and development of artificial intelligence and robot systems in general. *Cyberanimetrics* is the name I have given this field. Cyberanimetrics is the study of biological organisms and machines (largely theoretical at this point) that exhibit some or all of life's qualities, ie: organization, irrita-

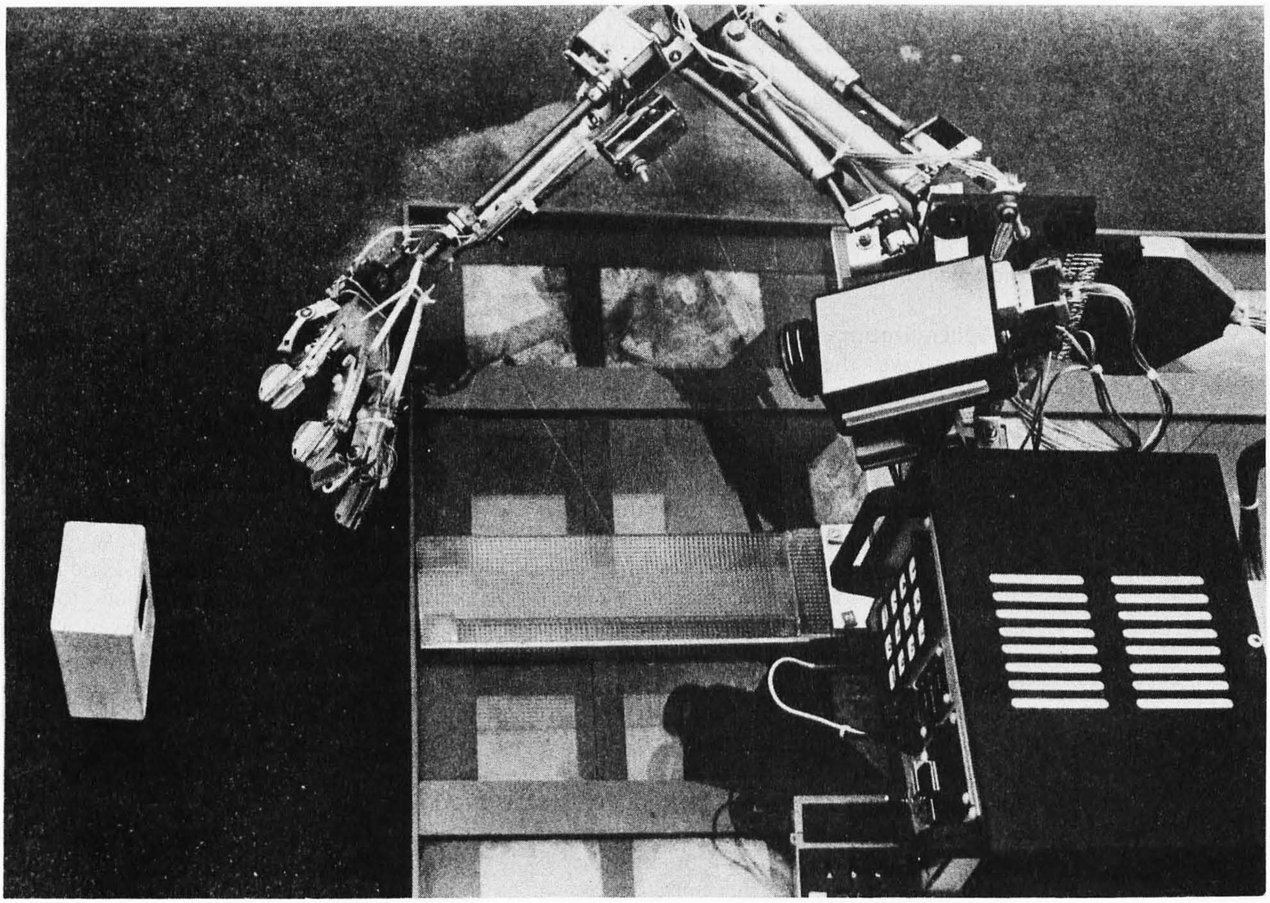


Photo 1: The author's robot arm and eye mechanism, modeled after the frog's insect catching mechanism. The eye uses a square array of light sensors that simulate the net convexity detectors found in the retina of the frog's eye, used by the frog to detect small, fast moving insects. The arm is similarly patterned after the frog's tongue and arm grasping and moving action. Construction of a portion of the eye mechanism is described in part 2 of this article.

bility, movement, growth, reproduction, and adaptation. These animate systems are studied from the standpoint of the information movement that is necessary for the system's operation or survival. Cyberanimetrics combines neural cybernetics and computer cognition with a host of other sciences to analyze both data flow and the structure where this data flow occurs. By studying biological and mechanical systems from this vantage, the designer becomes aware of the fact that the micro and macrostructures of both types of systems have to be specialized through either evolution or design, so that the system can operate successfully in its environment. Cyberanimetrics is, more than anything else, a study of system specialization.

Specialization through good organization is important in any robot or artificial intelligence system. But in the past it was thought to be more important to make the system as sophisticated as possible. Consequentially, many systems built were simply collections of unrelated but extremely advanced devices, making it very difficult for the early designs to operate as a system. It is not a major problem in robotics today to achieve complexity in a system; rather the problem has become how to make the complex systems operationally efficient and successful for a given end. Organization is important because one method can result in a much cheaper, more reliable, and less complex system. But to organize a system, the designer must first see how other systems are organized.

This is where cyberanimetrics comes in: instead of examining only the creations of engineers, the designer also examines nature's creations. This comparison of natural and artificial systems by the designer is quite logical since I feel that a robot or an artificial intelligence is an attempt by man to utilize certain physical or behav-

ioral design aspects of biological systems (ie: bionics). Cyberanimetrics allows the designer to appreciate the variety of methods employed by the various systems because both mechanical and biological systems are examined in terms of their similarities in structure and organization. This means that a person designing a system must be equally familiar with biology, computer sciences, cybernetics, artificial intelligence, mechanics, and physics.

Biological Considerations

Generalizations regarding the nervous system leave the impression that nerves merely conduct information, or that the eye works somewhat like a television camera that sends an inverted image to the brain for analysis. These oversimplifications might lead designers to believe that they can make a computer "see" by interfacing an array of digital light detectors to it. But, there is more to vision than meets the digital eye. In the compound eye of the ant, for example, there are 1200 *ommatida* (light sensitive elements). Some of these are so specialized that they are sensitive only to the polarization of ultraviolet radiation from the sun and are used by the ant exclusively for navigational purposes. Other ommatida are used for color, size, or motion detection and all are connected to the brain by nerve fibers that not only conduct but also process the video information. However, it is very doubtful that an ant "sees" an image in the sense of human consciousness; more likely, it apprehends its optical environment in some other way.

Just as important as being able to understand various biological and mechanical concepts is the ability to apply these concepts to the design of a system. After all, it would be impractical to try to build an authentic copy of an organism. In the previous example, if a neural cybernetist wanted to utilize digital light sensors, he might attempt to duplicate the ant's visual system. But, he would face many problems, the toughest being the construction of artificial ommatida. Each ommatida in the ant's eye has a particular structure depending on its function, whereas digital sensors are a matrix of uniform sensing elements. It would be very difficult to build the individual micro-optics necessary to perform color separation light polarization analysis. Of course, some of the analysis could be performed by a computer, but the more effort that goes into making a system into a faithful model of the ant, the more the system would be compromised. *In the end, it would have been more economical to use a real ant.*

If, instead of attempting to copy the ant like the neural cybernetist, or ignoring the ant like the cognitionist, the designer applies the concepts of ant vision toward a certain goal, he might stand a chance of developing an operational system. If the system is to navigate by sunlight, certain aspects of the ant's polarization detector would be useful; however, color recognition and motion detection would be useless features and therefore not included in the system. The purpose of cyberanimetrics as a design philosophy, then, is to intentionally apply accepted, standard biological and mechanical concepts to create a robot or artificial intelligence device that can accomplish certain predefined goals.

Cyberanimetrics and Design

To see how cyberanimetrics works as a design philosophy, consider the design of the system pictured in photo 1. This system, named NELOC (neural logic cyberanimate), was initially designed for use as a subsystem on a land survey vehicle (LSV). Built to be located in a forward turret, the system was designed to gather soil, liquid, and flora samples from its location. Ideally, the system could do this either automatically or by remote operator control.

The only critical limiting factor in the system's design is cost. To stay within a reasonable budget, I had to organize the manner in which I was going to design the system so my effort would not be wasteful or redundant. I resolved the matter by formulating the following steps for research and development:

1. Define the system's application.
2. Define the qualities necessary for the system to perform its application.
3. Based on these definitions, consider the mechanisms employed by biological or mechanical systems that closely match the definition.
4. Analyze the system(s).
5. Based on this analysis, evaluate the relative merits, (ie: cost, complexity, and performance) of using the analyzed system's method in the design of the robotic (in this case, turret) system. Translate this analysis into design.

These guidelines forced me to clarify the need for the system and the means and method of its operation — and I found that these five steps involving the system design were more important than the phases of its construction.

Design work on the system began by defining its characteristics. I determined

that the turret system should be able to locate, classify, and manipulate objects close to it (within reaching distance of the manipulator arm). To accomplish this, the turret system would have to exhibit four animate qualities. First of all, the turret system would have to be *organized* (ie: that the system had to be able to handle the movement and analysis of data in some consistent manner). The system would also have to express *irritability* (ie: certain stimuli, whether internal or external, would cause the turret system to act in some characteristic manner). For example, if a specimen moved out of the system's view, the system would respond by looking for the lost specimen. The third animate quality was *motion*, a necessary quality for the system to work in its environment. The last quality required is *adaptation*, probably the most important feature since I could not envision all of the possible situations the system might encounter. However, this type of adaptation would not be structural, but rather "intellectual" in nature. Without the ability to adapt, the system would not learn from failure.

After considering the proposed design characteristics, I selected the frog as a model to study, primarily because of its fascinating ability to locate and catch insects. In order to catch a flying insect, for instance, the frog must be able to scan an area greater than the reach of its tongue and then classify various objects such as prey, predators, other frogs, etc, based on sensory data. Finally, the frog responds to the flying insect (solely on the basis of visual information) by attempting to catch the object. Although the structures of the frog and the turret system are significantly different, the function in each case is similar.

The second reason for selecting the frog is simplicity. By selecting the frog over a more complex organism (ie: more highly evolved), I would save much time in determining a model of how the frog performed its functions. Figure 1 shows the frog and some of its main neurological constituents. The eyes and sensory neurons form input devices. The small lobular brain and spinal cord make up the bulk of the processing system, while the motor nerves and muscles serve as output mechanisms. This phase and the next involved quite a bit of work, since there was so much data to examine. It should be noted that the presentation of my analysis here is very abbreviated in order that most of the concepts can be discussed. One structure in particular, the net convexity detector, is given a more detailed treatment, however. The detector's function and structure will be discussed extensively, showing how the concept was researched and applied to the design of the turret system. This research and development is representative of the work performed on the entire system. A bibliography is provided in part 2 of this article for those who wish to research the subject more.

Optical Processes of the Frog

Analysis of the frog began with the sensory and motor nervous systems, in particular the eye. The frog's eye is classified as a camera-type eye, meaning that the entire image is focused through a single lens. The perception and subsequent analysis of an image begins on the surface of the retina. There, thousands of groups of receptors and their associated neurons capture tiny portions of the total image. After the retinal neurons process the receptor data, they communicate it to the optic nerve, which further processes the data as it is relayed to the brain. The result is the generation of four specific types of information about the image being perceived. The first type of information that the frog's nervous system extracts from the image is *net dimming*, which describes how much of an image has dimmed when compared to the previous image. *Moving edge* is the second type, concerned with motion at the periphery of objects in the image field. Next is *sustained contrast* data. This information relays the shape and size of an object in the image field by describing edges of optical contrast. Finally there is *net convexity* data. This data relays the speed and direction of relatively small objects.

Of the four types of data, the last two, sustained contrast and net convexity data, are probably most responsible for the location and definition of objects and, therefore, warranted a more detailed examination.

While searching for more information, I found a research project by J Y Lettvin, who researched amphibian vision at MIT (see bibliography). In his paper, he attributes net convexity and sustained contrast data primarily to the arrangement of the associated neuron's receptors on the retina. Lettvin also supports that a model in which net convexity data is generated by one configuration of receptors and neurons while sustained contrast is generated by another. The receptor/neuron group responsible for generating net convexity data (called a *net convexity detector*) is characterized by a broad field of low sensitivity receptors and a small cluster of high sensitivity receptors (see figures 1 and 2). The cluster of high sensitivity receptors is never located in the center or on the edge of the low sensitivity

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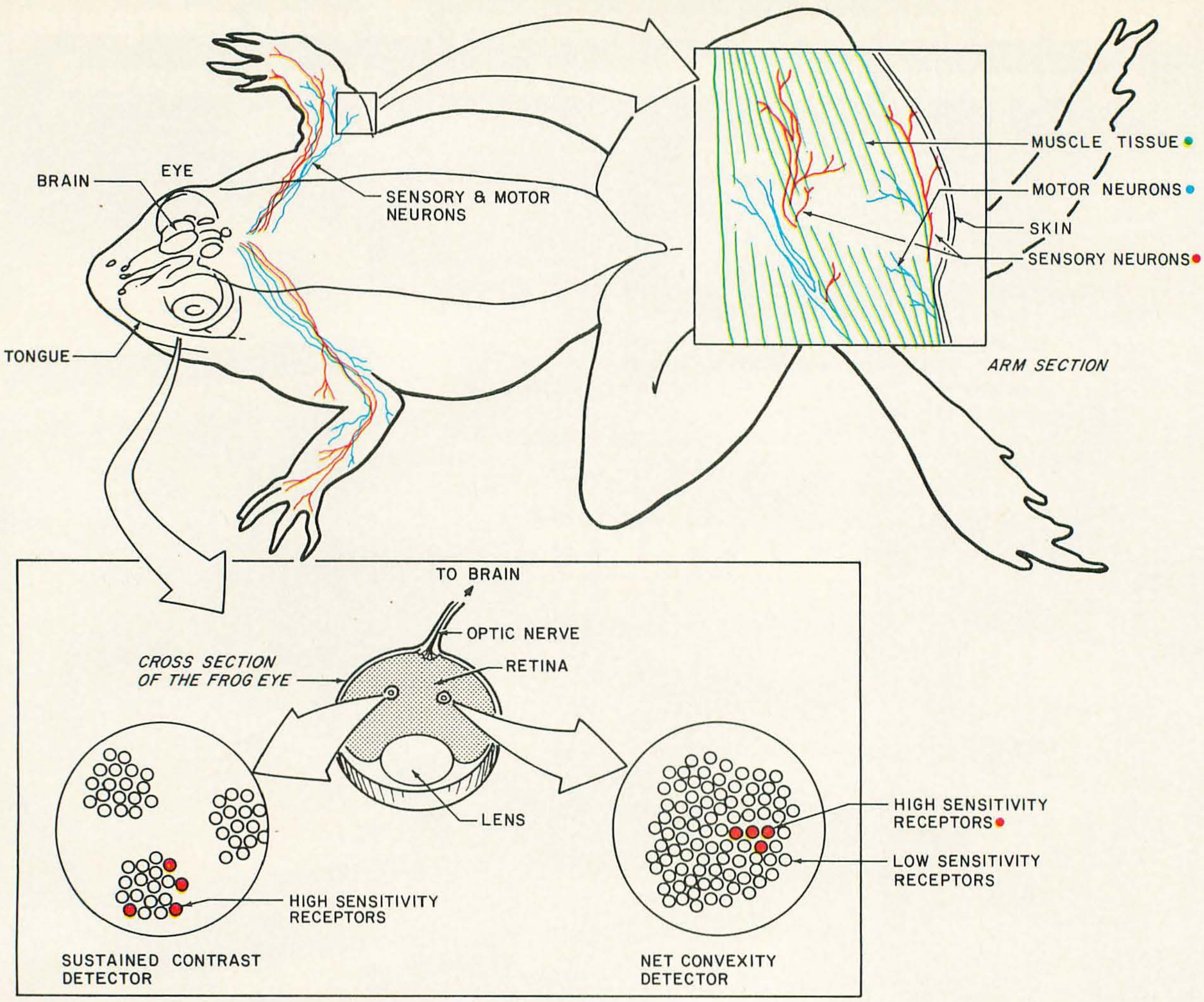


Figure 1: Some of the main neurological components in the frog. The frog's evolutionary success is due in part to certain structures in the eye and brain that have evolved for the specialized task of catching fast moving insects. Sustained contrast data (from the sustained contrast detectors shown) relays the shape and size of an object in the image field by describing edges of optical contrast. The net convexity detectors are used to uniquely determine the direction and speed of small, fast moving insects.

field, but rather somewhere in between. Apparently it is critical that the high sensitivity cluster be located in such an eccentric position because the neuron uses this cluster as a "landmark." This landmark helps the neuron generate a signal that the nervous system can decode into angle and direction information. *[The frog's retinal field is more complex and organized than that of the mammalian retinal field. However, this is because the higher vertebrates have relegated higher brain centers for visual, informational processing. For a discussion of this, see "What the Frog's Eye Tells the Frog's Brain," Lettvin, et al,* Proceedings of the Institute of Radio Engineers, *number 47, 1959, pages 1940-1951.]*

Net Convexity

From the receptor's aspect, the system works approximately as follows: as the prey's (ie: fly's) image falls upon the frog's retina, it transverses many groups of receptors. As the image triggers the first peripheral receptor of the net convexity detector, the neuron begins to "fire." From then on, as each low sensitivity receptor in that group is encountered, the voltage level across the neuron will increase. This higher voltage is always the sum of the previous "signal" plus the present signal. However, when a high sensitivity receptor is encountered, the neuron responds with an abrupt voltage transient, after which the voltage level returns to the next summed value. This means that if a fly's image were to cross a net convexity detector in such a way that it triggered the high sensitivity receptor, the resulting waveform, if viewed on an oscilloscope, would be a staircase with a transient "spike" located somewhere near the middle steps. Call this waveform A (see figure 2a). If another fly image were to cross the same net convexity detector but on a different angle that still crossed the high sensitivity cluster, the resulting signal (see figure 2b, waveform B_1) would look similar to waveform A; however, on closer inspection it can be seen that the number of steps and the position of the spikes are different.

To the frog's nervous system, this means that the vectors A and B_1 are uniquely

described by the number and type of receptors encountered by the moving image. The *number of steps* in the waveform (or the low sensitivity receptors encountered) describes the angle of the vector, while the *position of the spike* (or the location of the high sensitivity receptor) identifies the direction of the vector. This means that, as long as an image's trajectory crosses the high sensitivity cluster, the *associated neurons* can describe the image's vector of travel. For example, waveform A describes a vector that encounters three low sensitivity receptors and one high sensitivity receptor followed by one low sensitivity receptor in this retinal section. Decoded by the nervous system, the signal would mean that the insect was travelling diagonally left to right. If the spike had occurred between the second and third steps instead, the nervous system would have decoded the signal to mean that the insect was travelling on the same vector in the opposite direction.

The associated neuron plays a significant role in net convexity detection. The total surface area of the frog's retina is less than one quarter the area of a postage stamp: the actual net convexity detector is a microscopic structure. This means that an image moving across the retina could span a single group of receptors in a matter of microseconds. The associated neuron could require up to 5 μs (or more) to complete a firing cycle, meaning that several dozen receptors can be crossed by an image before the firing cycle (ie: transmission) of the

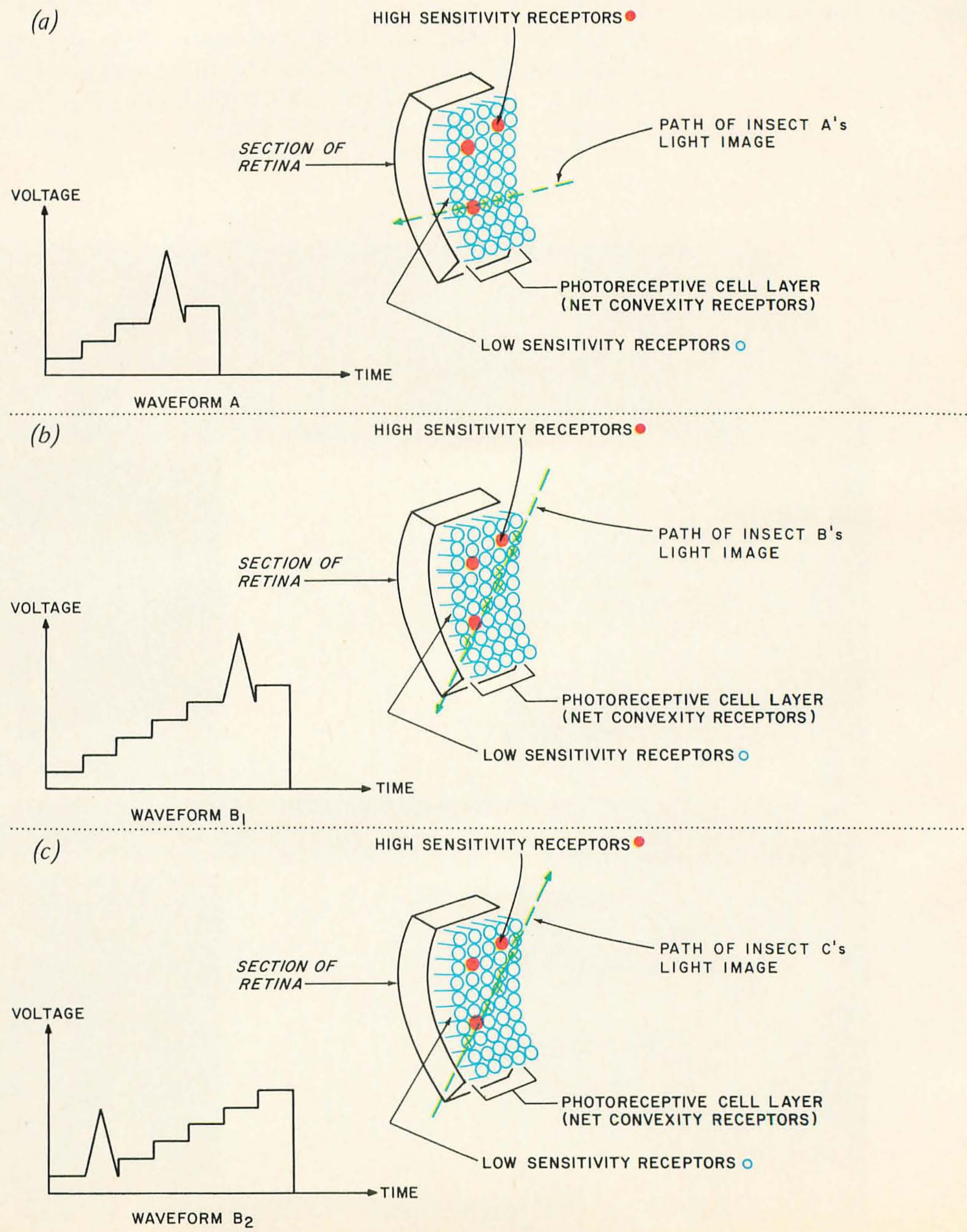
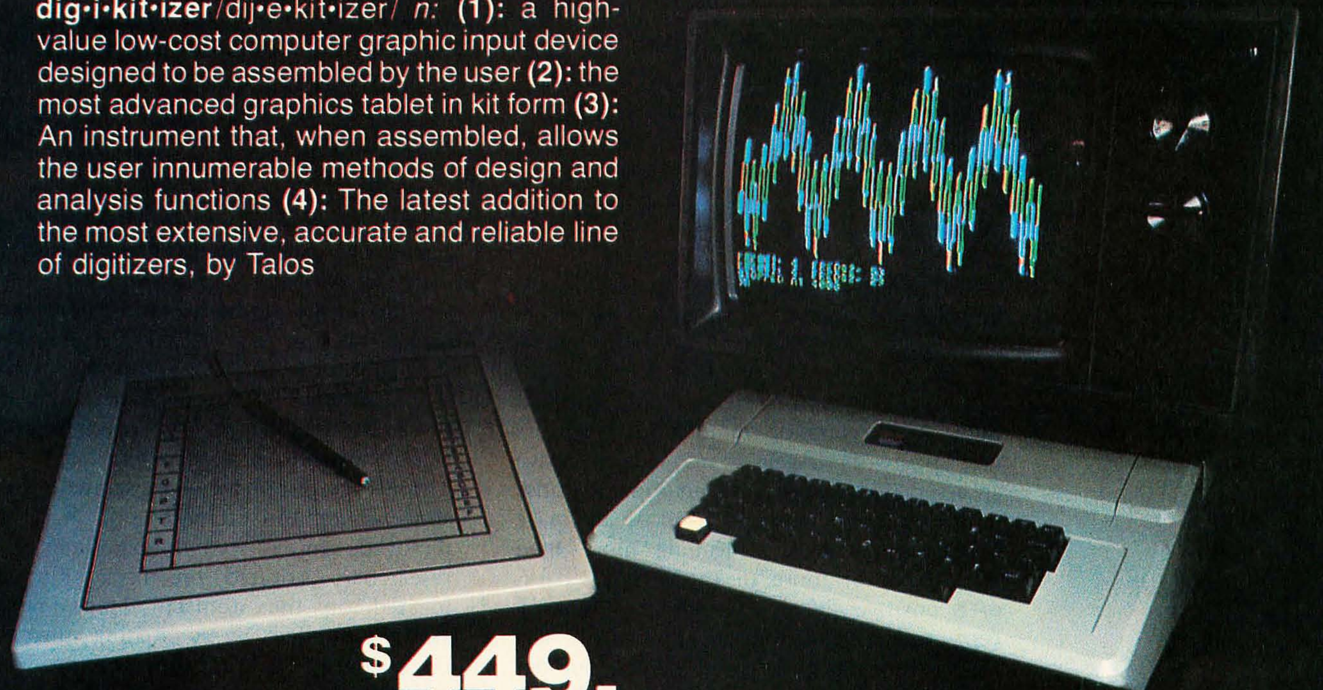


Figure 2: The net convexity receptor. As a fly's image crosses the retina, it traverses many groups of receptors. As the image triggers the first peripheral receptor of the net convexity receptor, the associated neuron begins to fire. Each additional low sensitivity receptor encountered adds to the cumulative voltage level. In addition, any high sensitivity receptor encountered causes the neuron to emit a transient voltage spike, as shown in figures a, b and c. The eccentric position of the cluster of high sensitivity detectors enables the brain to deduce both the magnitude and direction of the vector of travel by noting the relative position of the spike in the waveform (compare figures 2a and 2b). Figure 2a shows the path of a typical insect image passing a section of the frog's retina. Compare with figure 2b, in which the angle of travel and the resulting waveform are different. Figure 2c shows the effect of reversing the direction of travel shown in figure 2b.

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neuron is complete. This is why the waveform looks the way it does: the neuron will fire with constant duration so that, as the images travel at different velocities across the receptors, the length of the steps in the waveform will vary. The associated neuron does more than record the pattern and speed at which receptors are stimulated; it also has the ability to sort sizes. An image that can stimulate more than two receptors at a time will depress (ie: inhibit) the neuron's output. The depressed output is ignored by the nervous system. Therefore, the net convexity detector is a structure concerned with the angle, direction, and velocity of small, insect sized objects.

Sustained Contrast

Sustained contrast data, too, depends on receptor geometry as an aid in image processing, but not to the same extent as the net convexity detector. Instead, the sustained contrast detector is composed of a small group of homologous receptors (see figure 1). Again, the receptors have an associated neuron. This neuron's response to its receptor's interpretation of an image is either no signal, meaning more than 60 percent or more of the image is dark, or a positive signal, meaning that 60 percent or more of the image is light. The neuron's response is based on the number of illuminated receptors and is called a "majority response." When the majority responses of thousands of sustained contrast detectors are combined and processed by the optic nerve and lobe, the brain is provided with a sustained contrast image.

Tactile and Kinesthetic Senses

The next sensory systems I decided to examine were the frog's kinesthetic (ie: relative positioning of body parts) and tactile sensing "mechanism." Tactile sensation in the frog begins with specialized receptors located in the skin (see figure 3). These receptors are innervated capsules of tissue. The nerve endings within these capsules are the tips of large cutaneous nerves. All of the receptors contained in a certain tract of skin are merely branches of a single nerve ascending to the spinal cord. This means that a single nerve, as long as the frog's arm, can generate a signal that is recognized by the brain as location and pressure intensity data for literally hundreds of receptors.

Appendage position detection is similar to the tactile system. Again, a long nerve branches from the spinal cord. These branches terminate in special capsules called neuromuscular spindles. The neuromuscular spindles are special capsules of muscle tissue that have nerve endings coiled around them. As the muscle contracts, the spindle contracts, stimulating the nerve ending. Each skeletal muscle has many spindles within it (see figure 3). The brain decodes the signal to discover the number of spindles contracted, which describes the length of the muscle. The length of the muscle is indicative of the position of a joint.

How the brain can decode location and pressure data from a single nerve is not thoroughly understood; however it is thought that, during the frog's embryogenesis, the innervation of tissue is somehow recorded by the brain. This record serves as a template for the brain to use in the recognition of the origins of the signal. This was demonstrated in an experiment in which a young frog had a small portion of its stomach skin grafted to its back. The skin removed from its back was then grafted to the spot where the stomach skin had been removed. Some time after the grafts had healed, the researchers irritated the stomach skin on the frog's back. The frog responded by scratching the spot where the stomach skin had been removed. In a second experiment, the researchers irritated the back skin graft located on the stomach. This time the frog responded by scratching the graft on its back. The conclusion of the experiment was that the frog's brain had identified the location of the tissue by its innervation, and not by the path the signal took to the brain.

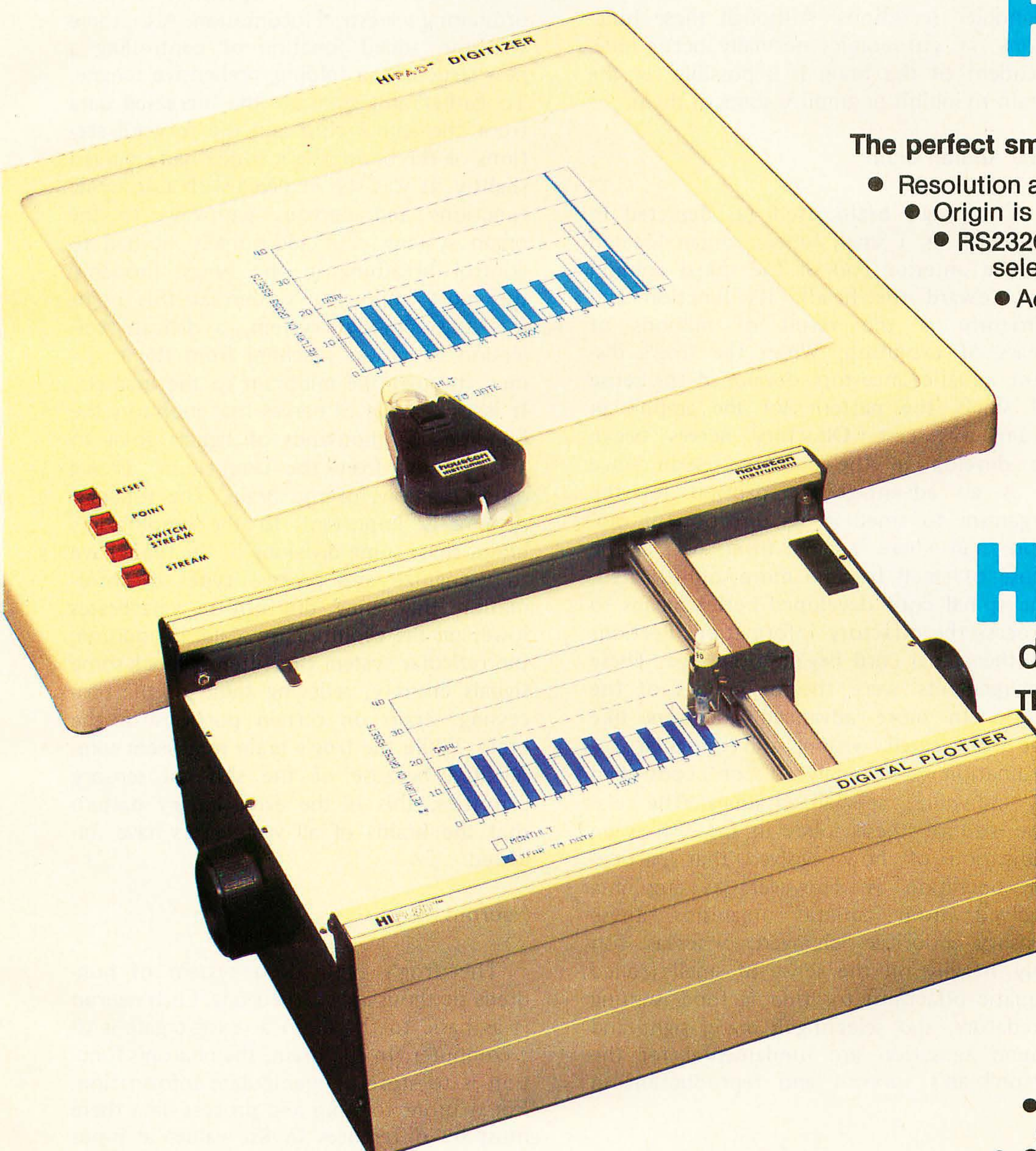
Motor Circuit

The motor circuit performs the opposite function of the appendage position and tactile sensory systems. Instead of gathering data about muscles, the job of the motor circuit is to carry the signals that stimulate the muscles. To stimulate its muscles, the frog has a set of specific nerves descending from its spinal cord and terminating in specialized muscle fibers. At these fibers (called neuromuscular junctions) signals leave the nervous system and enter the muscle tissue, stimulating muscular contraction.

For the signals to get to and from tactile, motor, and kinesthetic systems and the cerebellum (where motor patterns are stored), they must travel along the spinal cord. The primary function of the spinal cord is to relay the billions of bits of data to and from various neural pathways in the frog's body; it also performs various regulatory and control functions, ranging from reflex (such as the knee-jerk reflex

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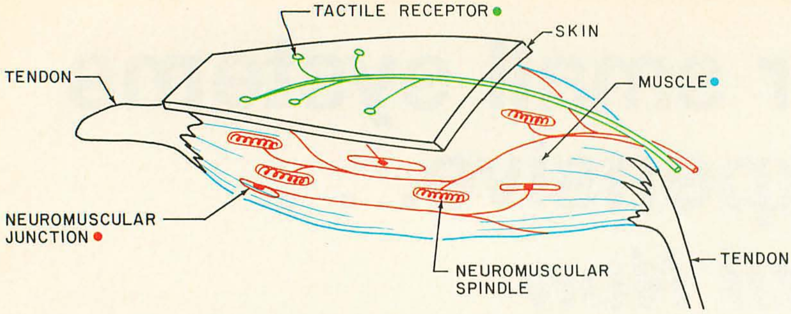


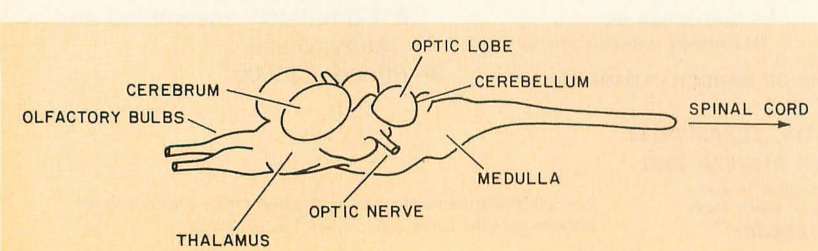
Figure 3: Section of muscle and skin showing portions of the tactile and neuromuscular (motor) systems of the frog.

in humans) to iris dilation and control of glandular secretions. Although these functions (ie: autonomic) normally occur independent of the brain it is possible for the brain to inhibit or amplify some of them.

The Anuran Brain

The frog's brain itself (as depicted in figure 4) is a small lobular organ located at the anterior end of the spinal column (ie: toward the head). Its function and structure is the result of millions of years of evolution. When the frog's distant aquatic ancestors developed the sense of smell, the pattern for the amphibian brain was cast. Olfactory nerves began to develop in the anterior region since it is an advantageous adaption for the organism to smell in its direction of motion than where it came from. And as the sense of smell became more sophisticated, the spinal cord developed better means to process the olfactory information. Portions of the spinal cord began to enlarge. These enlargements were the beginnings of the lobes. In more advanced ancestors like the fish, smell, vision, and muscular coordination are analyzed or controlled by individual, specialized lobes. The relative size of these lobes in the fish is an indication of how evolved that particular operation is. However, as amphibia evolved from aquatic organisms, these sensory priorities changed: whereas fish rely heavily on the sense of smell (called aquatic olfaction) for finding food, sensing predators, and selecting a mate, sight and sound sensation are fundamental for the amphibian's survival and reproduction in an amphibious (ie: semi-terrestrial) habitat. To accommodate the change in the order of significance of sensory data, the amphibian brain increased in size with functional and structural changes. Consequently, the thalamus and cerebrum, once exclusively olfactory "data processors," now began to process some optic and aural data.

Figure 4: The lobular brain of the frog. Note the large olfactory bulbs and the forebrain lobes. These structures are part of the frog's aquatic legacy.

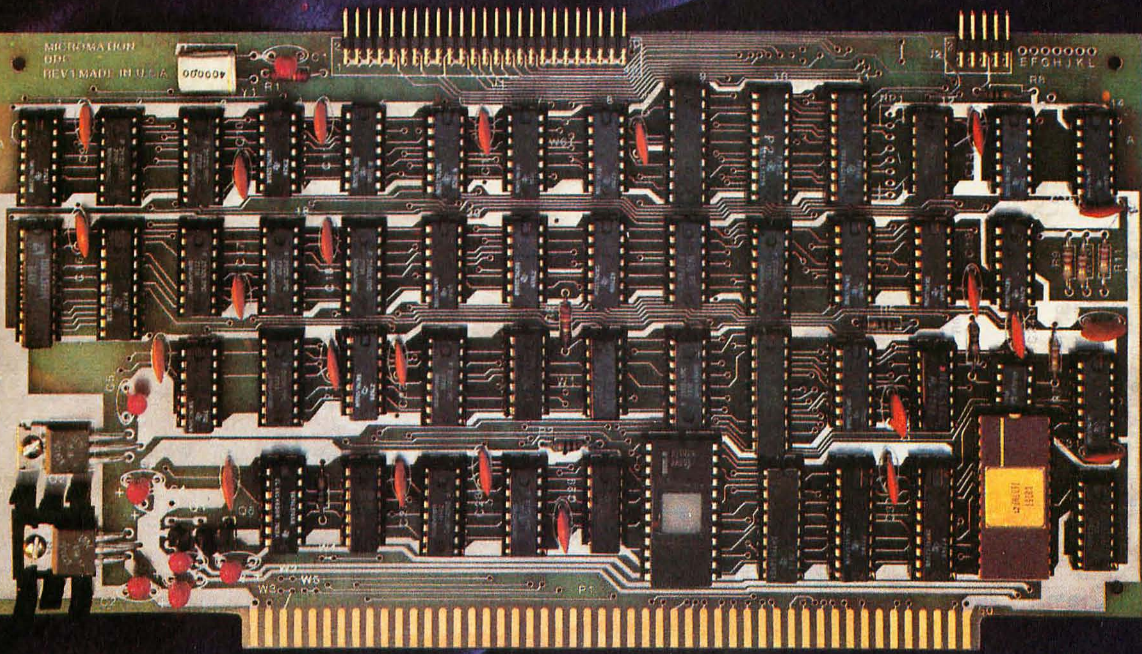


Other structures of the brain remained somewhat the same, although their importance too had changed. The cerebellum, which processes equilibrium information and produces the signals for muscular coordination, became responsible for coordinating terrestrial locomotion. Also, there was the added function of controlling a new structure—a folding, prehensive tongue. To gather and transmit the increased data from the spinal cord and the forward sections of the brain, the medulla had enlarged slightly. It was still involved with autonomic functions and nervous pathways to the organ systems, but additionally, it had to control breathing in the lungs. Probably the most important system at this point was the *reticular* system, a delicate collection of nerves reaching from the thalamus through the midbrain to the medulla. It is this group of nerves that monitors the hundreds of thousands of signals going to and coming from the cerebellum, among other portions of the brain. The reticular system is important to the amphibian's brain, since some divisions of the brain have to recognize and process types of information that they did not in vertebrates lower on the evolutionary scale. In addition, the reticular system can filter or block some signals entirely, relieving some of the processing strain on certain portions of the brain. While the frog's brain may seem complicated because of the shift of sensory priorities, this is the evolutionary pattern that the brains of all vertebrates have followed.

Neurons

The frog's brain is a system of hundreds of thousands of neurons. Each neuron is as basic to the brain as a logic gate is to a computer. In the brain, the neuron's function is to store or manipulate information. For neurons to store and process data there must be differences in the values at input or output junctions of the neuron. In the retina of the frog's eye, for example, the net convexity detector neuron generates a different type of signal for the high sensitivity receptor than for the low sensitivity receptor, as discussed earlier. It is only by such value assignments (called weighting) that neurons can store, process, or switch data.

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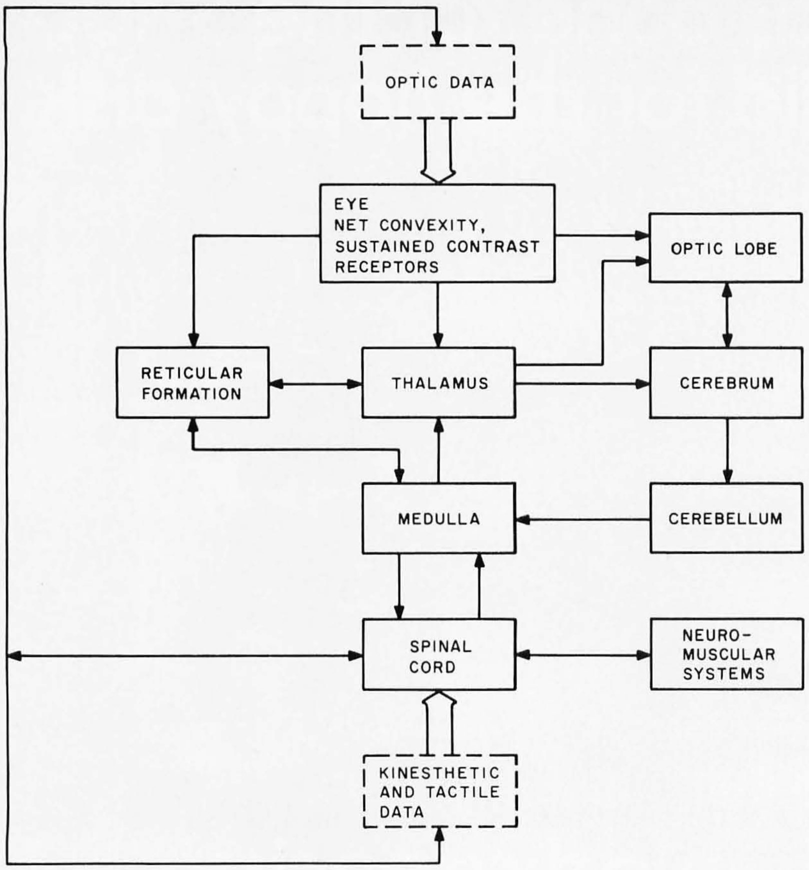


Figure 5: Simplified block diagram of the frog's insect catching "mechanism." The eye, tacile, and position sensory systems monitor the environment. Tactile and position data travel via the spinal cord to the medulla, where the reticular system alerts the thalamus. In the thalamus, sensory data is integrated and sent to other portions of the brain for processing. Finally, data goes to the cerebellum to be decoded into signals that will bring about coordinated motion.

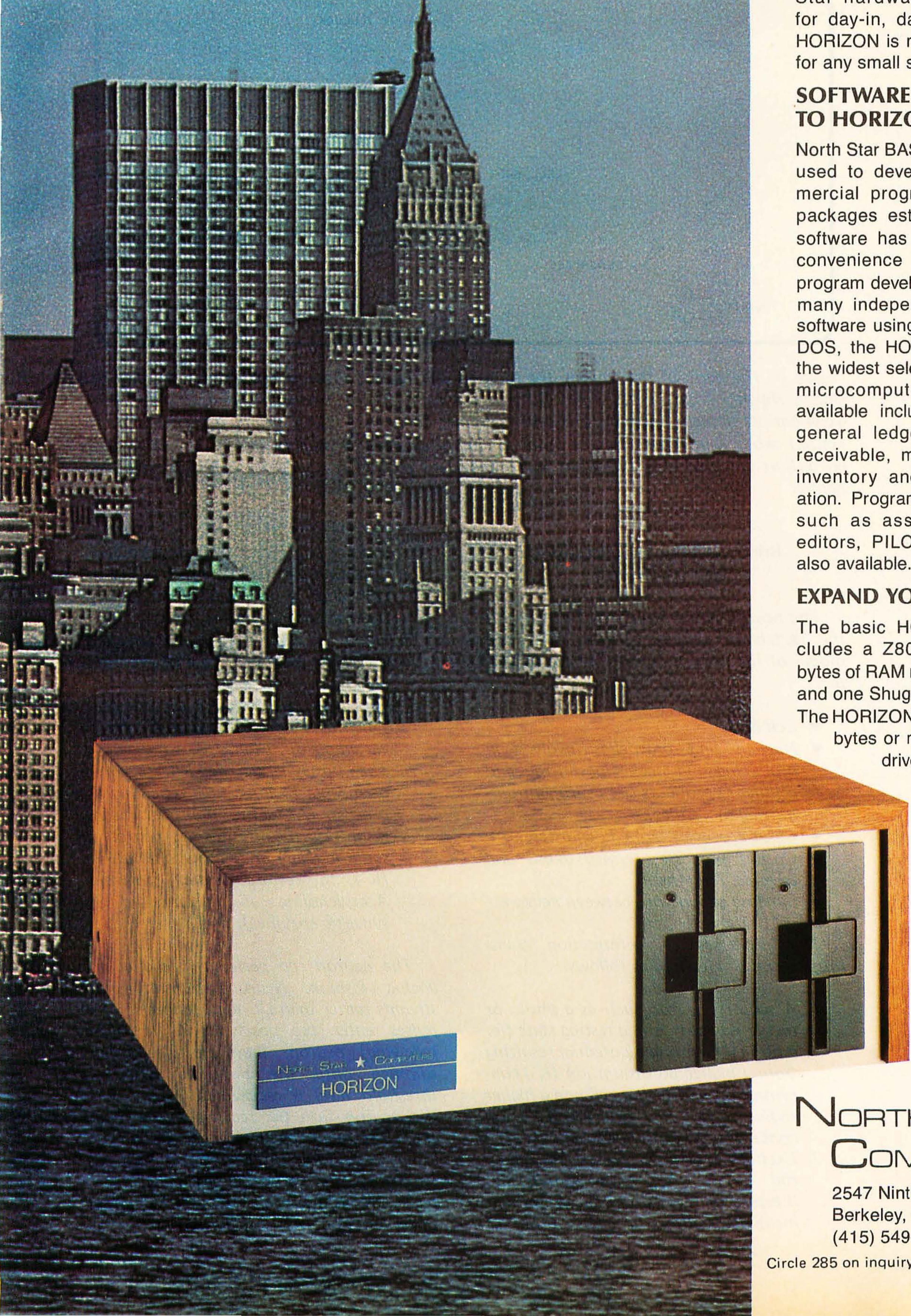
To illustrate this, assume that a frog had to "store" a single bit of data for three seconds. Using microscopic neurons with junctions end to end, three seconds of storage would require 1500 feet of neuron. If the frog had to store this quantity of data throughout its lifetime, its brain would be monumental in size. To save space, then, signals to be stored are channeled to a group of neurons that are "connected" in a chain by some of their inputs and outputs (called *axons* and *dendrites*, respectively). When data is introduced to the group, it is passed from one neuron to the next, forever looping until the pathway is somehow blocked. The other dendrites and axons of this group's neurons (a single neuron can have up to 1000 individual axons and dendrites) connect to other neurons that bring information to and from these groups. These neurons are electrochemically controlled. So, depending upon the electrochemical activity of the brain, virtually an infinite number of pathways can be realized. It is this type of operation (the opening and closing of pathways) that makes the brain function. This is a fundamental process of any algorithmic device. In a computer program, certain pathways are opened or closed depending on the status of the program or its data. In a calculator, certain logic pathways are opened or closed based on data in the system. This does not mean that a calculator and a frog's brain operate by the same mechanism, but only that the principles are the same.

To conclude this brief neurological model of the frog, I integrated my data into a coherent block diagram. Figure 5 represents the neurological and physical aspects of the insect catching mechanism. This system involves sensing optical and mechanical information from the environment. Light reflected from objects is analyzed by two methods: net convexity detection and sustained contrast detection provide the brain with size, shape, speed, and direction information. External pressure is monitored by tactile sensors. A second system of nerves with terminations deep in skeletal muscle and at skeletal joints is used to relay information about muscle length to the brain, which interprets this data to determine the position of its appendages. This data is transmitted to the brain by travelling from the spinal cord to the medulla. As the medulla passes the information along to the more forward sections of the brain, the reticular formation alerts the thalamus that data is on the way. In the thalamus, all types of sensory data are deciphered and compacted into precise neurodata statements, which are then dispatched to the cerebrum and cerebral cortex for processing. Some data is stored while other pieces are "copied," "deleted," "added to," "computed," etc. From the cerebrum new data will arise, some of it sent to the cerebellum. There the data is decoded into instructions concerning the motion of the frog. It is the job of the cerebellum to generate the signals that will bring about the coordinated motion of the frog. But for these signals to cause motion, they must travel to the muscles through the medulla, across the spinal cord, and finally to the various motor circuits. From the motor circuits the signals leave the nervous system and enter the muscle tissue, causing motion.

The NELOC System

This analysis may seem extremely impractical for use in hobbyist level robotics, but in fact it provided me with much of the inspiration I needed for the development of the *neural logic cyberanimate.* But it was possible to conceive and design these appliances only by understanding the nature of the operation of the frog's sensory systems. Part 2 of this series describes how a robot was built using the concepts described here. Some construction details for a portion of the eye mechanism are also given.

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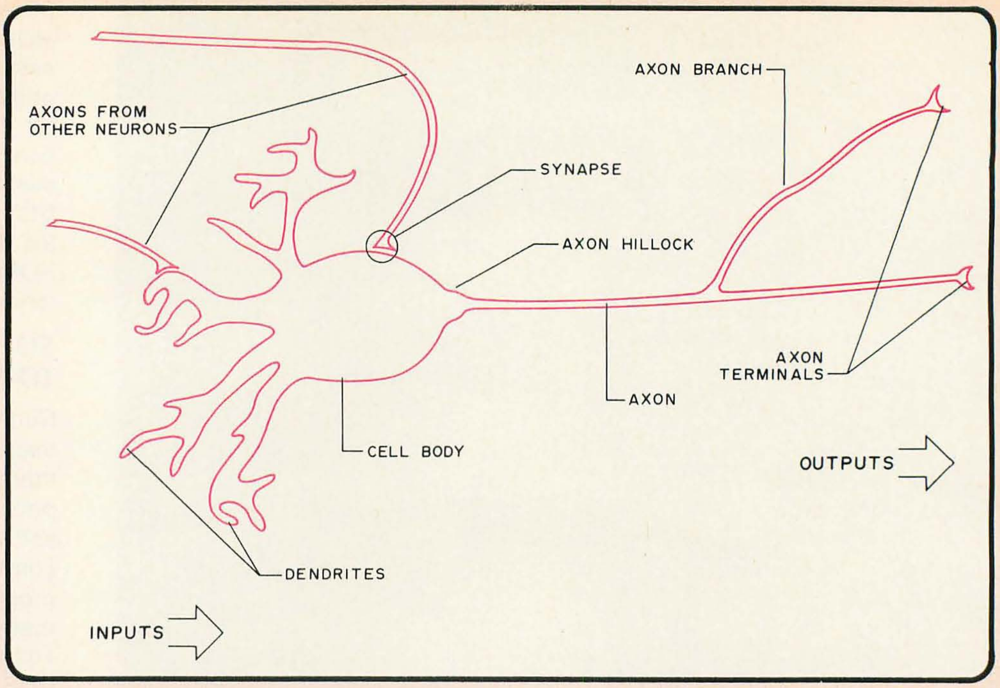


Figure 6: The parts of the neuron, the brain's basic "gate." Flow of information through this gate is roughly from left to right. Outputs are digital pulse streams transmitted through the axon and its branches to inputs of other neurons. Inputs are digital signals from other (presynaptic) axons, which are summed by an analog process which weights various sources and fires an output pulse when a threshold is reached. This neuron receiving input is termed postsynaptic.

Brief, but Essential Concepts of Neuronal Systems

The neuron is the basic unit (ie: gate) of the vertebrate nervous system. The ideal model of the neuron consists of the following:

- *Cell body.*
- *Nucleus and organelles involved in producing and packaging energy and cellular byproducts (ie: neuronal transmitting molecules).*
- *Input processes termed dendrites.*
- *Output processes termed axons and terminal boutons.*
- *Synapse or juncture between neurons.*

The processes of information transmission can be idealized as follows:

1. *A sensory neuron such as a photo or tactile receptor is in a resting state (ie: a 60 mV membrane potential resulting from a higher potassium ion (K^+) concentration within the cell and a higher sodium (Na^+) and chlorine (Cl^-) ion concentration outside the cell.*
2. *Excitation of this (presynaptic) neuron by its respective stimuli (ie: pressure or normally induced ion permeability) allows a great influx of sodium (Na^+) ions. This causes a depolarization (ie: action potential) in the cell and is transmitted as a wave phenomenon down the axon.*
3. *Upon reaching the axon's terminus, the signal induces release of the transmitting substance (ie: acetycholine). This neurotransmitter enters the postsynaptic neuron across the synapse via simple diffusion.*
4. *The postsynaptic dendrite becomes permeable to ions, thus repeating the process. (An active transport mechanism rids the presynaptic neuron of sodium (Na^+) and imports potassium (K^+) to restore resting potential. Acetylcholine is decomposed by synaptic enzymes).*

The neuron can perform in digital and analog fashion. Neurons transmit pulse streams rather than DC voltage levels: when pulses enter the postsynaptic (ie: signal receiving) neuron, they are algebraically summed until the threshold firing or threshold level is reached, at which point the neuron fires (ie: reaches action potential). The many factors that can enter into signal processing in the neuron (different weightings for various input signals, feedback arrangements, etc) allow it to perform differentiation and integration as well as

simulate the workings of AND gates, OR gates, operational amplifiers, and other devices. However, the neuronal output signals pulses are digital in character. That is, the action potentials of the axon resulting in neurotransmitter release are one shot, one way signals with discrete amplitude and duration. With this model of the neuron in mind, the robotics experimenter should consider some of the basic transmission mechanisms of vertebrate nervous systems:

- *The neuron can be stimulated to increase or decrease rate of signal transmission. Thus, neurons can encode information by pulse frequency modulation (ie: temporal summation of signals).*
- *Signals can be processed in terms of spatial summation of receptor locations, as in optical and tactile senses.*
- *Spontaneous activity (such as autonomic functions) may be a result of neurons with thresholds near resting potential levels—resulting in constant or easily initiated action potentials.*
- *Neuronal pools or ganglia have numerous organizational possibilities besides the myriad types of neurons they may employ. Some possibilities are facilitation, subthreshold stimulation of neurons by presynaptic neurons; convergence, many inputs on one neuron; divergence, one neuron sending inputs to many neurons; spatial selectivity and weighting, as in net convexity, and continuous excitation by a neuron receiving its own axonal branch.*

Notes on Neuromuscular Systems

The skeletal muscles of amphibians are composed of bundles of striated fiber cells encased in connective tissue septa. These cells have a fascinating microstructure too complicated to describe in depth for our purposes. Considering this, the essential components important to neuromuscular understanding are: a system of ion transporting tubules, a septum surrounding the cell (with ion/molecule supplying capillaries imbedded in the septum) and protein fibrils running longitudinally to the muscles and perpendicular to the tubules.

The fibrils' tiny constituents are what contract to change muscle length. These are myofibrils (1-2 μm long) — protein rods which are arranged in overlapping rows and contract in a sliding, ratchet-like motion upon influx of calcium (Ca^+) ions for which they have an affinity. The tubules hold and transport the calcium ions.

Neuronal action initiates the entire process as follows:

1. *An action potential reaches the terminal end of a motor neuron's axon imbedded beneath the fiber cell membrane.*
2. *Acetylcholine is released from the neuron causing increased permeability of the fiber's membrane to calcium ions.*
3. *This condition increases until a propagated wave is sent across the entire muscle fiber resulting in myofibril contraction.*
4. *The acetylcholine is enzymatically catabolized and the resting potentials resume.*

Neuronal action detects contraction via neuromuscular spindles (dendrites and specialized fibers encapsulated in common tissue). These receptors detect the degree of fiber stretch (ie: depending on myofibril ratchet position) in a comparative way. The spindle receptor has a resting potential associated with its resting shape. Fiber stretch deforms the spindle, increasing the receptor membrane's ion permeability. This fires the receptor when threshold is exceeded.

The Golgi tendon organ is a kinesthetic receptor located at the muscle/bone junction. These receptors detect muscle tension, not muscle stretch, as do spindles.

The spindle receptor actually consists of primary, secondary and gamma receptors. The primaries produce large numbers of signals upon slight muscle stretches. Thus, primaries detect rate of change of muscle action by frequency pulse modulaton. The secondaries are capable of signalling length of muscle information because they require a longer period (in milliseconds) to reach threshold and action potential. Thus, secondaries transmit a steady state signal for information of a different quality than that of the primaries. The following references contain excellent discussions of neuronal functions in terms of biological and robotics concepts. . . . DWH ■

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3. Kent, Ernest W, "The Brains of Men and Machines, Parts 1, 2 and 3," January, February, March 1978 BYTE, pages 11, 84 and 74.
4. Sampson, Jeffrey R, *Adaptive Information Processing, An Introductory Survey*, Springer-Verlag, New York, 1976.

Part 2 concludes this article with details on building the robot eye and arm mechanism. The author's complete bibliography will also be provided in March 1979 BYTE.

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A Microprocessor

Part 2: Instruction Set Dead Ends,

Terry Ritter and Joel Boney
Motorola Inc
3501 Ed Bluestein Blvd
Austin TX 78721

In part 1 of this series (see January 1979 BYTE, page 14) we discussed the instruction set and other details of the Motorola 6809 processor. Part 2 is a question and answer discussion of the design philosophy that went into the 6809.

Any change from old to new inevitably brings criticism from someone. Indeed, any failure to change to include someone's pet ideas brings its own criticisms. We have not been isolated from sometimes severe criticism, nor from its political implications.

However, a number of our decisions have been reasonably challenged, and here we hope to present illumination and defense. While we are aware of a number of improvements which might have been included, the whole point is to sell a reasonably sized (and thus reasonably priced) integrated circuit. We hope that architectural errors of commission, as they are found, will be seen in light of the complete design. We are not aware of any such errors at this time.

Point 1:

The replaced instructions (PSHA/PULA, TAB/TBA, INX/DEX) all take more cycles and bytes than before. Why did you do such a thing?

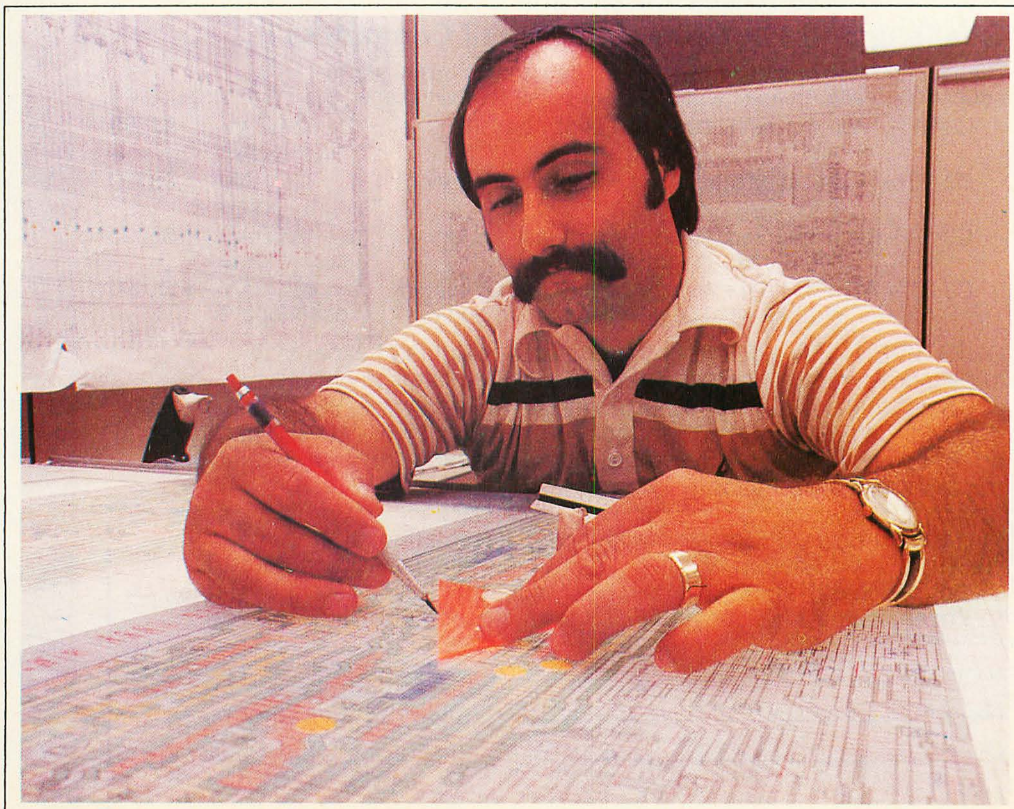


Photo 1: Layout. Layout designer Tony Riccio adds a line in a large layout cell. The various colored lines represent different types of conductors (metal, polysilicon, N+, etc) which will be formed on the integrated circuit. (The yellow dots represent problems to be corrected.)

for the Revolution: The 6809

Old Trails and Apologies

Answer 1:

Consider: the question is not just PSHA/PULA, but rather PSHA/PULA/PSHB/PULB/PSHX/PULX/PSHY/PULY/PSHU/PULU, *etc*, as well as similar op codes for the other stack. *There are only 256 1 byte op codes.* If the PUSHs and PULLs are made 1 byte, others must be made 2 byte, and *these* will take more cycles and bytes than before. And the macrosequenced PUSH or PULL instructions are *more efficient* than 1 byte op codes when more than one register is involved.

Similarly, as more registers are added, the number of possible transfer paths become combinatorially larger. Do you really want to give up that number of 1 byte op codes?

As for INX/DEX, we find that these were frequently used in 6800 code because they were more convenient than any other alternative. We now offer autoincrementing and autodecrementing indexing as a viable (ie: shorter, in cycles and bytes) alternative. We also allow arbitrary additions to X, Y, U and S.

Point 2:

I don't see any facility for expanding the 64 K address space.

Answer 2:

True. Memory expansion is possible, but consider this: microprocessors are products of a mass production technology –

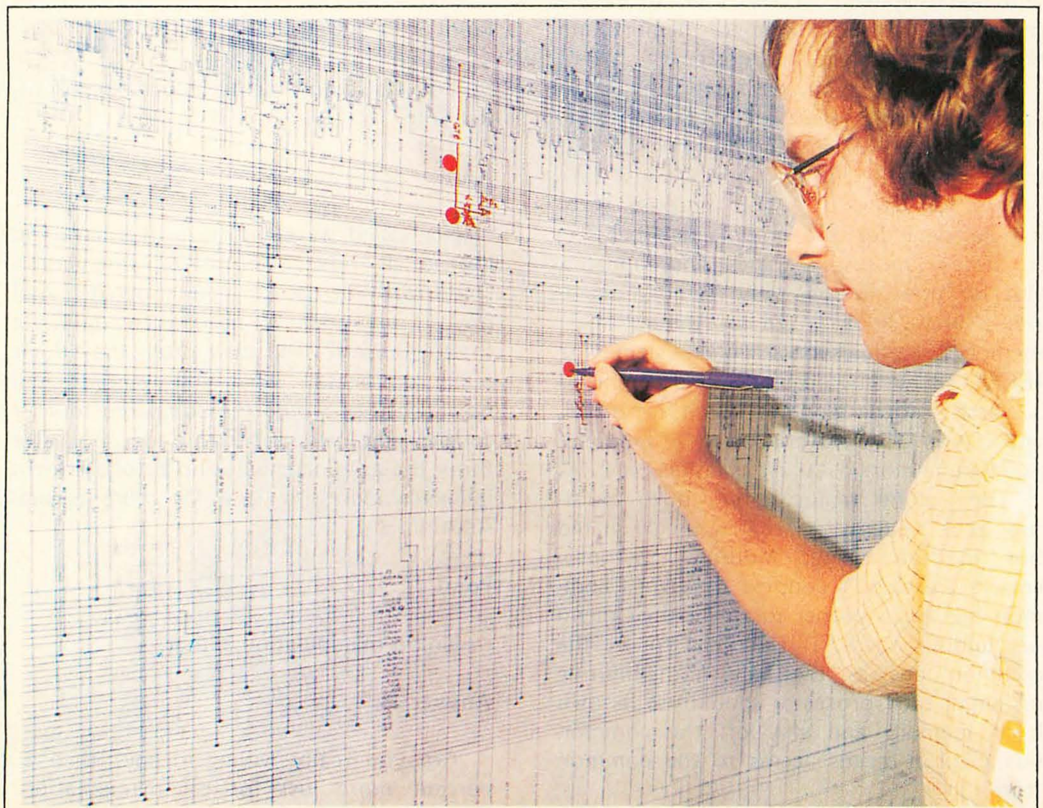


Photo 2: Breadboard design. After partitioning the logic, the MOS (metal oxide semiconductor) diagram is translated to TTL. The required ten boards are then designed and built. Meanwhile, Bill Keshlear updates the logic changes on the master copy of the logic diagrams, since they will imply changes on the boards.

processor cost is no longer a system limiting factor. It is generally inappropriate to use a single \$20 processor to control \$10,000 worth of memory; the single processor could use only a fraction of the bandwidth resource available in that much memory (here, bandwidth means the maximum possible rate of change of storage state under processor control). A far more reasonable approach is to place the same total store on ten processors and give yourself the possibility of major throughput improvement. Naturally you'll have to learn how to control all this power, but if you're an innovative systems designer, that's exactly your job.

There are two principal divisions of multiprocessor systems, depending on the degree of coupling between the processors. Closely coupled processors usually communicate through some common memory; loosely coupled processors communicate through input/output ports, serial lines, or other "slow" communications channels. Loosely coupled systems can usually be understood as networks of quasi-independent processors.

Now, let's consider a concept that we call "smart memory." One reason for wanting more address space on a processor is to randomly access a large store of on line data. Most of your processing is spent cataloging data, storing data, moving, searching and updating data. If you want to handle more data, you put on more memory and the system gets bigger and slower.

But suppose you put a processor on each reasonable piece of memory (16 K or whatever). Make the program for that processor really dumb – make it just take orders for data. Its whole purpose is to handle data for the command processor; it stores, moves, searches and updates. But for now, it does only memory operations. Now hook a lot of these "smart memory" modules onto your system (the IEEE 488 bus should work), and command a search. All the modules search in parallel, and if you grow and put on more modules, you handle more data just as fast as ever!

The second major approach to multiprocessor systems is what we call shared bus multiprocessing. Multiple microprocessors are closely coupled through a common bus and a proper subset of their memory address space. It is crucial to see the common bus as the bandwidth limiting resource; each processor should use its own local memory and stay off the common bus until it needs access to the common store.

Multiple requests for common memory access might be issued by various processors at exactly the same moment. It is therefore necessary to arbitrate among them, switching exactly one processor onto the common bus, and allowing it to proceed with its memory access while the others are held *not*-READY.

It should be clear that the same concept (a common bus arbitration and switching node) can be hierarchically extended. Further, the addressing capability can be expanded and possibly remapped at each node to allow fast random access to huge amounts of on line mass storage. Such obvious extension is left as an exercise for the serious student. Perhaps you are thinking that you *can* build it, but nobody can write the software to control it. We are not insensitive to the problem, just unhappy with the attitude. We worked hard to give you the tool; all you have to do is learn to use it. Every new technology is like this – our scientists still don't know how to fully control the atom, but that doesn't stop atomic fusion from being one of the most attractive "games" around since the payoffs are huge.

Nobody has a *chance* to develop complex multiprocessor software until she or he has a real multiprocessor system. Now, for \$500 and a little work, you've got the hardware. It's time to start learning to control these systems. If it's hard one way, do it another. The power is there for use.

Point 3:

You still didn't include block operations, did you?

Answer 3:

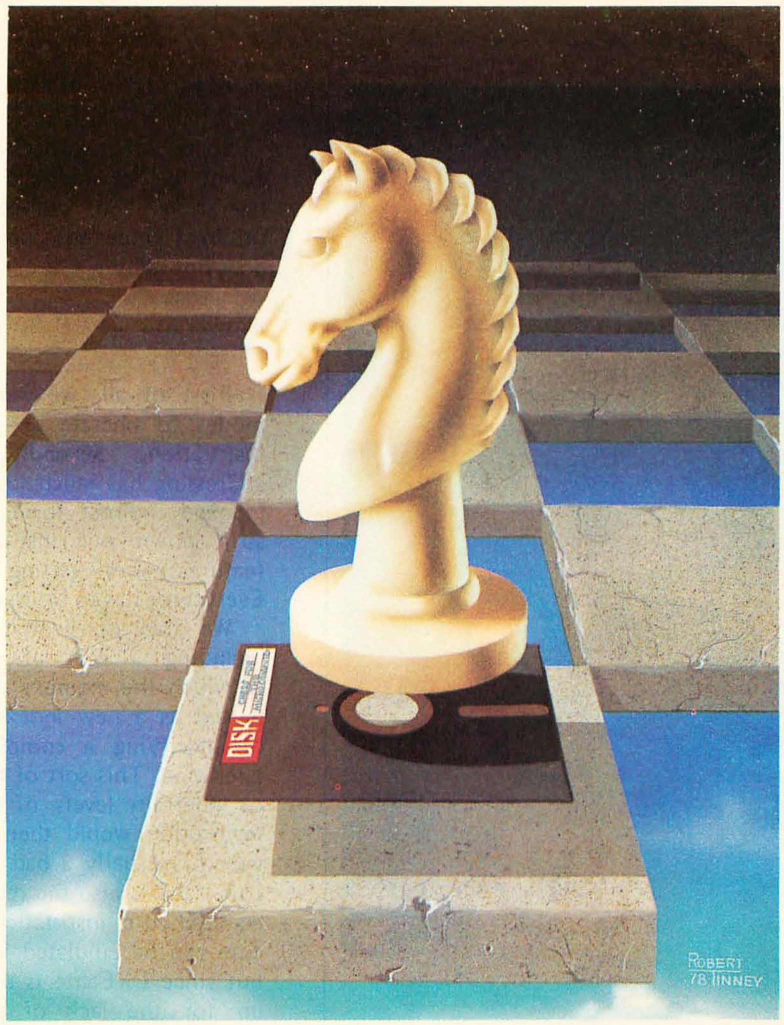
No – and we could have. But have you looked at how often block instructions could really be used in your programs? And how much code is needed to duplicate them yourself? And how often they don't really do exactly what you wanted? And how fast they would run compared to your programmed version? Please do look. We think the autoincrement and autodecrement indexed addressing is a far more general solution.

Point 4:

No bit manipulation, either.

Answer 4:

Are you really willing to pay 10 to 20 percent more just for bit manipulation? Program coded bit manipulation takes a



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Photo 3: Visual inspection. Some of the gross processing errors or problems that occur with probing equipment can be detected visually. Here, lead production operator Mary Celedon checks a 6802 wafer.

little longer, but is more general, and probably is located in a very lightly used portion of your program, thus having very little effect on your total throughput or program size.

Point 5:

Why no undefined op code trap?

Answer 5:

Because the machine is a random logic implementation. The unused op codes are used as "don't cares" in derivation of internal logic equations, thus allowing reduced logic and integrated circuit size. Failure to include the don't cares in the logic equations would result in a larger and more expensive circuit.

Point 6:

Some other processors allow both indexed before indirect (indexed indirect) operation and indirect before indexed (indirect indexed) operation, but yours does not. Why?

Answer 6:

First of all, we wanted our addressing modes to operate on all of our memory instructions. Secondly, indirect indexed addressing has much lower utility than our indexed indirect form. Thirdly, we didn't strip down our instruction set, so real features were getting a little precious. Everything has to fit on one chip, remember.

We had considered the possibility of including a sort of chained addressing, in which the memory data would be interpreted as a new indexed postbyte capable of specifying a complete new addressing operation. This sort of thing could continue to indefinite levels, of course. But such an instruction would then be executing data, which is usually a bad idea (self-modifying code) and is also the reason why we include no EXEcute instruction. (Naturally, EXEcute can be emulated if you really need it, but since EXEcute is usually used to make up for the lack of powerful addressing modes, it will not likely be missed from the 6809). Furthermore, this executed data would almost certainly be discontiguous in the memory space, making even the analysis of the simple case (read only memory) programs extremely difficult. Placing such an uncontrollable gimmick in a processor design would be like placing a glittering knife in front of a baby, and would be similarly irresponsible.

Point 7:

You have a MULtiply, but no DIVide.

Answer 7:

True enough. Multiply operations are required in high level language subscript array calculations, but how often do you really need divide? Do you really want to pay for something you will rarely use and can do easily with a program? Additionally, the unsigned multiply is easily capable of extension into multiple precision arithmetic. (Try that with a signed multiply!) Divide does not decompose as nicely. This, combined with the absence of similar instructions in the machine (divide needs

24 bits of parameters, both in and out) was enough to leave it out.

Point 8:

Your registers are all special purpose.

Answer 8:

Well, in a way, as we have 16 bits of accumulator and 64 bits of usable pointers plus some others. This basic dichotomy of data and pointers to data exists in practice, and is therefore rarely a problem with our implementation. But the EXG instruction allows convenient manipulation between these groups in any unusual circumstances.

Point 9:

Why did you include all those new addressing modes? I'll never use them.

Answer 9:

We expect that you *will* use the new addressing modes, and quite heavily. There are a lot of different indexed options. But notice that the large number of different modes is a result of including all permutations of a few basic ideas.

Fundamentally, you can index from any pointer register (x 4), use indexed indirect access (x 2), and have accumulator offsets (x 3) or constant offsets of up to 16 bits in three versions (x 3) (see box at lower right). But if you work in assembly language, you don't need to figure addresses, so the different constant offset modes may be ignored. And if you select an addressing mode which is not available, the assembler will politely inform you of your indiscretion.

Alternately, you can specify autoincrement or autodecrement operations (x 2), by either one or two (x 2), which may be indirected (x 1.5) (except there is no indexed autoincrement and autodecrement by one indirect – think about it). Finally, constant offsets are allowed from the program counter (x 3) and these may also be indirected (x 2).

There are a lot of modes, no doubt about it. But relatively few new ideas are required to gain full control over those powerful new features.

Point 10:

I would have liked an operating system call instruction which carried a parameter to the operating system.

Answer 10:

So would we. Unfortunately, the location I want to use for parameters may not (and probably will not) be what you want to use. It is desirable to allow both constant and variable parameters to the operating system. What you do get is two more trap-like software interrupt (SWI) instructions; the instructions SWI2 and SWI3 do not mask interrupts as SWI does, thus allowing use even in interrupt driven programs. Parameters may be passed in any register, or on the stack, or as the next byte of in line code. All of this will require some overhead, but the scheme is far more general than a trap that carries a parameter.

Point 11:

Tell me again about the stack pointers: why *two* stack pointers?

Answer 11:

Good point. The original reason for adding the user stack pointer was to facilitate the creation of a data stack in memory that is separate from the program stack. This avoids one of the serious problems of using a second generation processor in a modular programming environment – that of returning parameters to a calling routine. We want to pass parameters in a position independent manner, of course, but the return from subroutine (RTS) instruction uses the top element of the stack as a return address, and this address is placed on the stack *before* the subroutine is entered. On the 6800 there will be a lot of stack rearrangement going on to get around this problem. The user stack pointer was created as a new stack unencumbered with return addresses (or interrupt state information) to allow data to be passed between routines of different levels in a reasonable manner. And since the new stack works exactly like the old, there is relatively small silicon cost involved.

We do suspect, however, that many programmers will elect to accept the overhead involved with passing parameters on the hardware stack (note that the overhead problem is greatly reduced with the 6809). These programmers will be concerned with the access of parameters placed on the stack by higher level routines. Notice that, as more elements are added to the stack, these *same parameters* are referred to by *varying offsets* with respect to the stack pointer itself: this is bad, since it becomes difficult to analyze exactly which value is

The notation (x n*) means there are* n *ways to perform that particular operation. (x 1.5) means there are two ways to perform that operation but not every addressing mode is allowed. . . .*RGAC



Photo 4: Editing the layout. Drafting manager Wayne Busfield and senior layout designer Rick Secrist make changes indicated by engineering analysis. This iterative process improves performance and production yield, and thus lowers cost.

being accessed by any given subroutine. Thus many programmers will use the U register as a *stack mark* pointer, fixed at some previous location of the stack pointer. All lower level modules will then be able to refer to the same data by identical offsets from the U register.

Point 12:

Why do the 6809 stack pointers point to the last item on the stack rather than the next free location, as on the 6800?

Answer 12:

This architectural change was virtually mandated by following the chain of logic that resulted from extending the 6800 into double byte, autoincrement and stack indexable operations.

First, let us assume the above extensions with a 6800 style stack: the stack pointer thus points one byte below (lower in memory) the last byte deposited. Naturally the other pointers should work similarly (allowing their use as additional stacks, and requiring no new understanding). This means that the autoindex operations have to be preincrement and postdecrement. Now, suppose we have a stack or table of double byte data; the data pointer must be set up one byte *below* the data to prepare for autoincrement (or pull) operations. To access the first value, the expression LDD ,+S must be used, while succeeding operations appear to need LDD ,++S. This result is not great for loops. Alternately, the stack pointer could be made to point *two* bytes above the stack for double byte data only. This would require different offsets from the stack pointer (to access, say, the top of the stack) depending upon the size of the data being accessed. Different offsets would also be required, depending on whether the data was just being used,

or being pulled from the stack. This is workable, but not great conceptually. Another possibility is to form the effective address from the value of the pointer after only the *first* increment. This "kluge" solution would be hard to implement anyway, so we changed the stacks.

This chain of reasoning is an example of the difference between architectural design and just slapping instructions together.

Point 13:

Why not have more registers?

Answer 13:

Good designs are often the results of engineering compromises. To meet product size goals, only so many things can go on an integrated circuit. You can have registers, *or* features, or some combination. The 6809 does have approximately 20 addressing modes.

Registers for the sake of registers amount to little more than separate, very expensive and restricted memory areas. The register resource is always insufficient to hold temporary results in a large program, and must be reallocated in various routines. This allocation process is an error prone programming overhead. A separate register set for interrupt processing is suitable only for one interrupt level and, otherwise, is mostly wasted.

A few registers fully supported by features are better than just having a lot of registers.

Point 14:

Why no instructions to load or store the direct page register?

Answer 14:

The direct page register is one of those possibly dangerous features which was just too good to pass up (in terms of substantial benefits for minimum cost). The benefits include an operation length reduction of 33 percent for instructions using absolute addressing and a concurrent throughput increase of 20 percent. It now becomes possible to optimize code, perhaps allowing an oversized program to fit within discrete read only memory boundaries. The direct page register may also be used in a multitasking environment to allow single copies of routines to operate with multiple independent processes. However, providing a separate stack area and having each routine store local values on the stack may be a better solution,

Because a number of 6809 instructions (eg: INC/DEC, ASL/ASR/ROL/ROR/LSL, TST/COM/CLR/NEG) operate directly on memory, the direct page area may be used very much like a processor with 256 8 bit registers to hold counters, flags and serial information. So, perhaps most importantly, the direct page register relaxes the system requirement for programmable memory at a particular location (page 0) to use direct addressing; the cost is a single 8 bit register and no new instructions.

The programmer is cautioned to tread carefully when using the direct page register. All forms of absolute addressing for



Photo 5: First silicon engineering analysis. Logic and circuit design engineer Bob Thompson tracks down a weak node in the first batch of 6801 chips. The 6801 die is packaged, but not sealed, so that internal nodes may be probed while in operation. Viewing through the microscope, a probe can be placed at critical points equivalent to the layout plot. The chip itself is running a modified EXORcisor system, and the scope actually displayed an internal signal with excessively slow rise time.

Table 1: 6809 instruction set.

8 BIT OPERATIONS

Mnemonic	Description
ABX	Add B register to X register unsigned.
ADCA, ADCB	Add memory to accumulator with carry.
ADDA, ADDB	Add memory to accumulator.
ANDA, ANDB	And memory with accumulator.
ANDCC	And immediate with condition code register.
ASLA, ASLB, ASL	Arithmetic shift left accumulator or memory.
ASRA, ASRB, ARS	Arithmetic shift right accumulator or memory.
BITA, BITB	Bit test memory with accumulator.
CLRA, CLRB, CLR	Clear accumulator or memory.
CMPA, CMPB	Compare memory with accumulator.
COMA, COMB, COM	Complement accumulator or memory.
DAA	Decimal Adjust A accumulator.
DECA, DECB, DEC	Decrement accumulator or memory.
EORA, EORB	Exclusive or memory with accumulator.
EXG R1, R2	Exchange R1 with R2.
INCA, INCB, INC	Increment accumulator or memory.
LDA, LDB	Load accumulator from memory.
LSLA, LSLB, LSL	Logical shift left accumulator or memory.
LSRA, LSRB, LSR	Logical shift right accumulator or memory.
MUL	Unsigned multiply (8 bit by 8 bit = 16 bit).
NEGA, NEGB, NEG	Negate accumulator or memory.
ORA, ORB	Or memory with accumulator.
ORCC	Or immediate with condition code register.
PSHS (register)$_0^8$	Push register(s) on hardware stack.
PSHU (register)$_0^8$	Push register(s) on user stack.
PULS (register)$_0^8$	Pull register(s) from hardware stack.
PULU (register)$_0^8$	Pull register(s) from user stack.
ROLA, ROLB, ROL	Rotate accumulator or memory left.
RORA, RORB, ROR	Rotate accumulator or memory right.
SBCA, SBCB	Subtract memory from accumulator with borrow.
STA, STB	Store accumulator to memory.
SUBA, SUBB	Subtract memory from accumulator.
TSTA, TSTB, TST	Test accumulator or memory.
TFR R1, R2	Transfer register R1 to register R2.

16 BIT OPERATIONS

Mnemonic	Description
ADDD	Add to D accumulator.
SUBD	Subtract from D accumulator.
LDD	Load D accumulator.
STD	Store D accumulator.
CMPD	Compare D accumulator.
LDX, LDY, LDS, LDU	Load pointer register.
STX, STY, STS, STU	Store printer register.
CMPX, CMPY, CMPU, CMPS	Compare pointer register.
LEAX, LEAY, LEAS, LEAU	Load effective address into pointer register.
SEX	Sign extend
TRR register, register	Transfer register to register.
EXG register, register	Exchange register to register.
PSHS (register)$_0^8$	Push register(s) onto hardware stack.
PSHU (register)$_0^8$	Push register(s) onto user stack.
PULS (register)$_0^8$	Pull register(s) from hardware stack.
PULU (register)$_0^8$	Pull register(s) from user stack.

temporary values and parameters present problems in the development of large programs. Attempts to enlarge the number of direct locations by manipulating the direct page register may be tricky. And manipulation of the register by subroutines may lead to errors which switch the calling routines direct page in remote (ie: subroutined) unobvious code. Therefore, this register is made deliberately difficult to play with. Typically, it should be set up once and left there. To load the direct page register you can proceed as follows: EXG A,DP; LDA #NEWDP; EXG A,DP. Alternately, the direct page register is also available in PUSH/PULL instructions, but misuse is discouraged through lack of LDDP and STDP.

Point 15:

You preach consistency, yet you give us LEA, an instruction with different condition codes for different registers. Why is this so?

Answer 15:

The Z flag is unaffected by LEAS or LEAU, but conditionally set by LEAX or LEAY depending on the value loaded into the register. This provides 6800 compatibility with INX/DEX (implemented as LEAX 1,S or LEAX −1,X) and INS/DES (implemented as LEAS 1,S and LEAS −1,S), respectively.

Now clearly, if most 6800 programs are going to run on the 6809, the use of INX/DEX for event counts must be recognized. But in 6809 programs, releasing local stack area before executing RTS will be a very frequent action (LEAS −9,S; RTS) "cleaning up the stack." You do want to return a previous condition code value undamaged by the LEAS, so you get two types of LEA.

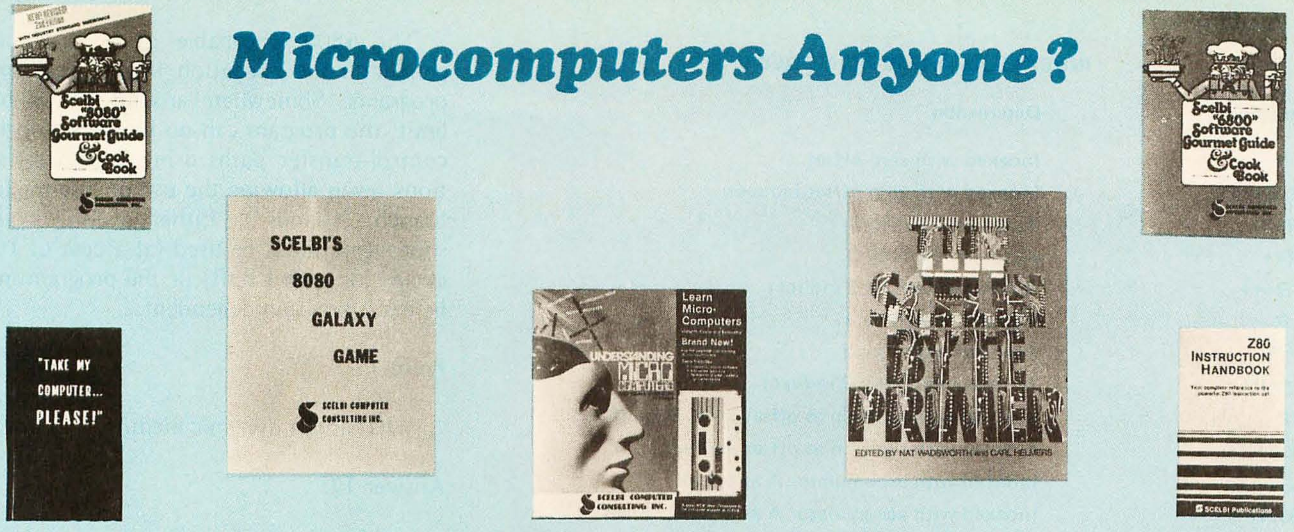
Point 16:

What about position independent code? Doesn't the 6800 allow it, too?

Answer 16:

Position independent code is one crucial factor in achieving low cost software. (Position independent temporary storage and input/output must also be available.) Only read only memories which may be used in arbitrary target systems are economically viable in the context of mass production. And only these read only memories can result in low cost firmware for us all.

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Table 1, continued:

INDEXED ADDRESSING MODES

Mmemonic	Description
0, R	Indexed with zero offset.
[0, R]	Indexed with zero offset indirect.
, R+	Autoincrement by 1.
, R++	Autoincrement by 2.
[, R+++	Autoincrement by 2 indirect.
, -R	Autodecrement by 1.
, --R	Autodecrement by 2.
[, --R]	Autodecrement by 2 indirect.
n, P	Indexed with signed n as offset (n=5, 8, or 16 bits).
[n, P]	Indexed with signed n as offset indirect.
A, R	Indexed with accumulator A as offset.
[A, R]	Indexed with accumulator A as offset indirect.
B, R	Indexed with accumulator B as offset.
[B, R]	Indexed with accumulator B as offset indirect.
D, R	Indexed with accumulator D as offset.
[D, R]	Indexed with accumulator D as offset indirect.

Note: *R = X, Y, U, or S; P = PC, X, Y, U, or S. Brackets indicate indirection. D means use AB accumulator pair.*

6809 RELATIVE SHORT AND LONG BRANCHES

Mnemonic	Description
BCC, LBCC	Branch if carry clear.
BCS, LBCS	Branch if carry set.
BEQ, LBEQ	Branch if equal.
BGE, LBGE	Branch if greater than or equal (signed).
BGT, LBGT	Branch if greater (signed).
BHI, LBHI	Branch if higher (unsigned).
BHS, LBHS	Branch if higher or same (unsigned).
BLE, LBLE	Branch if less than or equal (signed).
BLO, LBLO	Branch if lower (unsigned).
BLS, LBLS	Branch if lower or same (unsigned).
BLT, LBLT	Branch if less than (signed).
BMI, LBMI	Branch if minus.
BNE, LBNE	Branch is not equal.
BPL, LBPL	Branch if plus.
BRA, LBRA	Branch always.
BRN, LBRN	Branch never.
BSR, LBSR	Branch to subroutine.
BVC, LBVC	Branch if overflow clear.
BVS, LBVS	Branch if overflow set.

6809 MISCELLANEOUS INSTRUCTIONS

Mnemonic	Description
CWAI	Clear condition code register bits and wait for interrupt.
NOP	No operation.
JMP	Jump.
JSR	Jump to subroutine.
RTI	Return from interrupt.
RTS	Return from subroutine.
SEX	Sign extend B register into A register.
SWI, SWI2, SWI3	Software interrupts.
SYNC	Syncrhonize with interrupt line.

The 6800 is capable of position independent code execution in relatively small programs. Somewhere around a 4 K byte limit, the program can no longer support all control-transfer paths using branch instructions (even allowing the use of intermediate branch "islands"). Either a long branch subroutine must be used (at a cost of 100+ cycles for each LBSR) or the program must be made position dependent.

Point 17:

What about dynamic memory?

Answer 17:

There are two problems associated with dynamic memories: address bus multiplexing and refresh. Address bus multiplexing is the most severe problem but requires multiplexing 6+6 address lines (for 4 K memories) or 7+7 lines (for 16 K memories); these values are particularly inconvenient for 8 bit processors (which usually multiplex address/data). Thus, we have yet to see a processor address this problem.

Microprocessors that automatically refresh memory during most unused bus cycles waste power on unnecessary refreshes and unnecessarily increase bus activity. The 6809 can easily refresh dynamic memory in software (a timer causes interrupt execution of of FCB $10 63 times, then RTI), or can support hardware refresh (a direct memory access [DMA] sequence, or isolated board automatic refresh) at minimal cost.

Point 18:

What about price?

Answer 18:

The 6809 will be more expensive than in-production second generation 8 bit designs. For one thing, it is bigger and also new — both reasons imply reduced yield compared to older parts. A moderately higher price should not be a problem, since the processor cost is a very minor part of the price of a whole system. The total 6809 system should be nearly as powerful and much less expensive than 16 bit designs. The cost of not using the 6809, on the other hand, will likely be severe in terms of increased programming error rates, larger read only memories and decreased throughput.

In "Part 3: Final Thoughts" (March 1979 BYTE), we will conclude this series with a discussion of clock speed, timing, condition codes and software design philosophy.■

BYTE's Bugs

Tic-Tac?

Our apologies to anyone who entered the Tic-Tac-Toe program in "Tic-Tac-Toe in BASIC," by Mike Stoddard (December 1978 BYTE, page 174) only to find that part of the program was not there. Line 2580 obviously should not have been the last line of the program. Listing 1 is the missing section of program.■

Listing 1: Missing portion of Tic-Tac-Toe program.

```
2590     IF J=J1 GOTO 2610
2600  NEXT J1
2610  LET N=N-3
2620  FOR I1=1 TO 3
2630     LET N=N+3
2640     IF I=I1 GOTO 2660
2650  NEXT I1
2660  ON N1 GOTO 1440, 1710, 1730, 1760, 2670, 2970
2670  PRINT TAB (7); "I WILL PUT AN X IN BOX"; N;" YOUR TURN."
2680  LET L[8]=N
2690  GOSUB 2990
2700  IF F=1 GOTO 2690
2710  LET L[9]=L1
2720  LET N2=5
2730  GOTO 2400
2740  LET M=3
2750  LET K3=5
2760  GOTO 1890
2770  REM GAME STATE PRINT SUBROUTINE
2780  PRINT
2790  FOR I=1 TO 3
2800     FOR J=1 TO 3
2810        LET G$[0]=" "
2820        LET G$[J*3-2]=" "
2830        LET G$[J*3-1]=" "
2840        IF K[I, J]=1 LET G$[J*3]="0"
2850        IF K[I, J]=4 LET G$[J*3]="X"
2860        IF K[I, J]=9 LET G$[J*3]="-"
2870     NEXT J
2880     PRINT "\215\ ";G$[3];
2890  NEXT I
2900  PRINT "\215\"
2910  GOTO 1070
2920  PRINT TAB (7); "ILLEGAL INPUT. PLEASE ENTER AGAIN."
2930  GOTO 2950
2940  PRINT TAB (7); "WE HAVE ALREADY USED BOX"; L1;" PICK ANOTHER ONE."
2950  LET F=1
2960  RETURN
2970  PRINT TAB (7); "YIPPIE !!!!! I WIN WITH AN X IN BOX"; N
2980  GOTO 2780
2990  INPUT L1
3000  LET F=0
3010  LET L1= INT (L1)
3020  IF L1<1 GOTO 2920
3030  IF L1>9 GOTO 2920
3040  FOR I=1 TO 9
3050     IF L[I]=L1 GOTO 2940
3060  NEXT I
3070  RETURN
3080  END
```

Zapper Bug

I noticed a design error in "Zapper" (December 1978 BYTE, page 100) that would make the circuit quite difficult for the newcomer to troubleshoot.

The schematic shown on page 102 uses a 27 k ohm resistor as the "pull-down" of the program pin of the 2708. This is in direct conflict with the Intel book entitled *Memory Design Handbook*, copyright 1977. Pages 8 and 9 state that a resistive pull-down should not be used because the low level voltage

Continued on page 65

BYTE's Bits

TRS-80 Printer Use Hint

Many users of the Radio Shack TRS-80 microcomputer have found the optional line printer to be a useful companion for their processor. When the user adds the printer and the expansion interface unit to the Level II equipped processor unit, the hardware is ready to be used for applications, but the software must still be prepared. A useful kluge (ie: crude method which works during a transition period) to speed program conversion in making use of the printer has been developed by Vance James and Richard Bley of Hickory NC.

The Level II BASIC statements which cause data transfer to the printer are LLIST and LPRINT. They correspond to LIST and PRINT, which cause data to appear on the video display. It is possible to reverse the functions of these commands under program control. With reversed function, LIST causes programs to be printed on the printer, and PRINT causes data to be printed. LLIST and LPRINT would then produce output on the video screen and on the printer (in the reversed state, *everything* appears on the printer, as everything normally appears on the screen).

The program statements which reverse the keyword functions are as follows:

```
A=PEEK (16422)
B=PEEK (16423)
C=PEEK (16414)
D=PEEK (16415)
POKE 16414,A
POKE 16415,B
POKE 16422,C
POKE 16423,D
```

The above statements must of course have line numbers, but numbers may be supplied at the time this routine is incorporated into a program. After these statements are executed, the role of the video driver routine in the monitor and the role of the printer routine are interchanged. To return to a normal state under program control, the interchanging statements may be executed once more. . . .RS■

TSA Software Address Change

In the November 1978 What's New section of BYTE (page 216), we reported on disk based software development tools from TSA Software. We have recently been notified of an address change. Their current address is: 39 Williams Dr, Monroe CT 06468.■

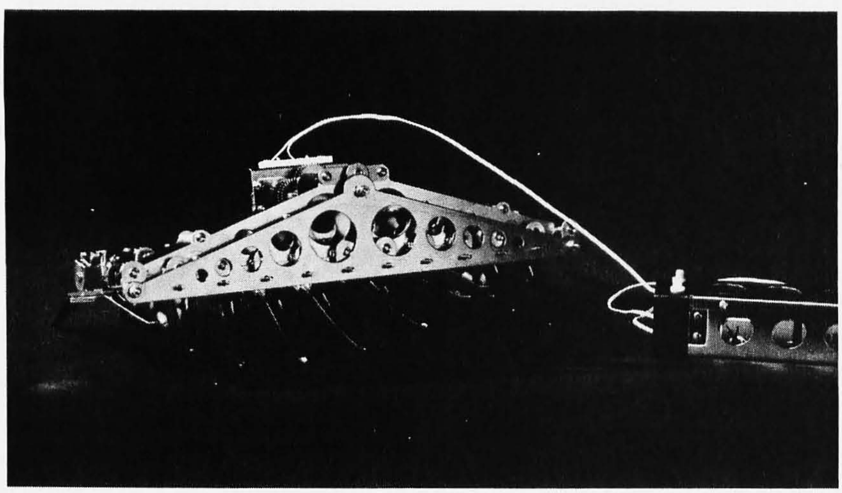
Mechanical Insects?

People interested in robot mechanics should know about Space Mechanimals which are built by a Japanese firm called GAKKEN. These all metal devices come in several shapes and sizes ranging from the 4 legged to the 20 legged beasty in photo 1 called a Giant Astro Centipede. This particular kit contains everything necessary to construct a 13 inch mechanical centipede. Even though the mechanism can only move forward and backward in straight lines the mechanism used to control the 20 legs is worth studying.

The Mechanimal kits use 2 D cells as a power source. I have found some trouble powering the kit from batteries since there is a large current draw. The actual assembly takes two to three hours and is recommended for people 10 years and older.

Anyone interested in robotics should peruse these devices to see how the motion is derived. I definitely feel that the centipede model was well worth the $39 that I invested in it. For further information about Space Mechanimals contact PIFC Importers, Portland OR, who are the exclusive importers of the devices. . . .RGAC■

Photo 1: Space Mechanimal.



Use Your Television Set as a Video Monitor

Timothy Loos
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Athens OH 45701

About the Author

Timothy Loos is presently finishing his PhD work in electrical engineering at Ohio University, where he is studying the interference effects of high powered FM broadcasting stations on air navigation receivers. His master's thesis consisted of a design for a video display for a minicomputer. Currently, he is using his TRS-80 system as an intelligent remote terminal, and for digital signal processing and communication systems simulation.

The main problem encountered using a standard television set as a high resolution video monitor is its limited bandwidth. The IF (intermediate frequency) sections, sound trap circuitry, and video amplifiers all limit the bandwidth of the signal to be displayed. An RF (radio frequency) modulator used with an unmodified television set forms a system capable of displaying a signal of up to 3.5 MHz bandwidth.

Feeding the video signal directly to the video amplifier of the set is helpful. Cutting out the sound traps also helps, but extending the bandwidth any further requires that major modifications be made to the video amplifier.

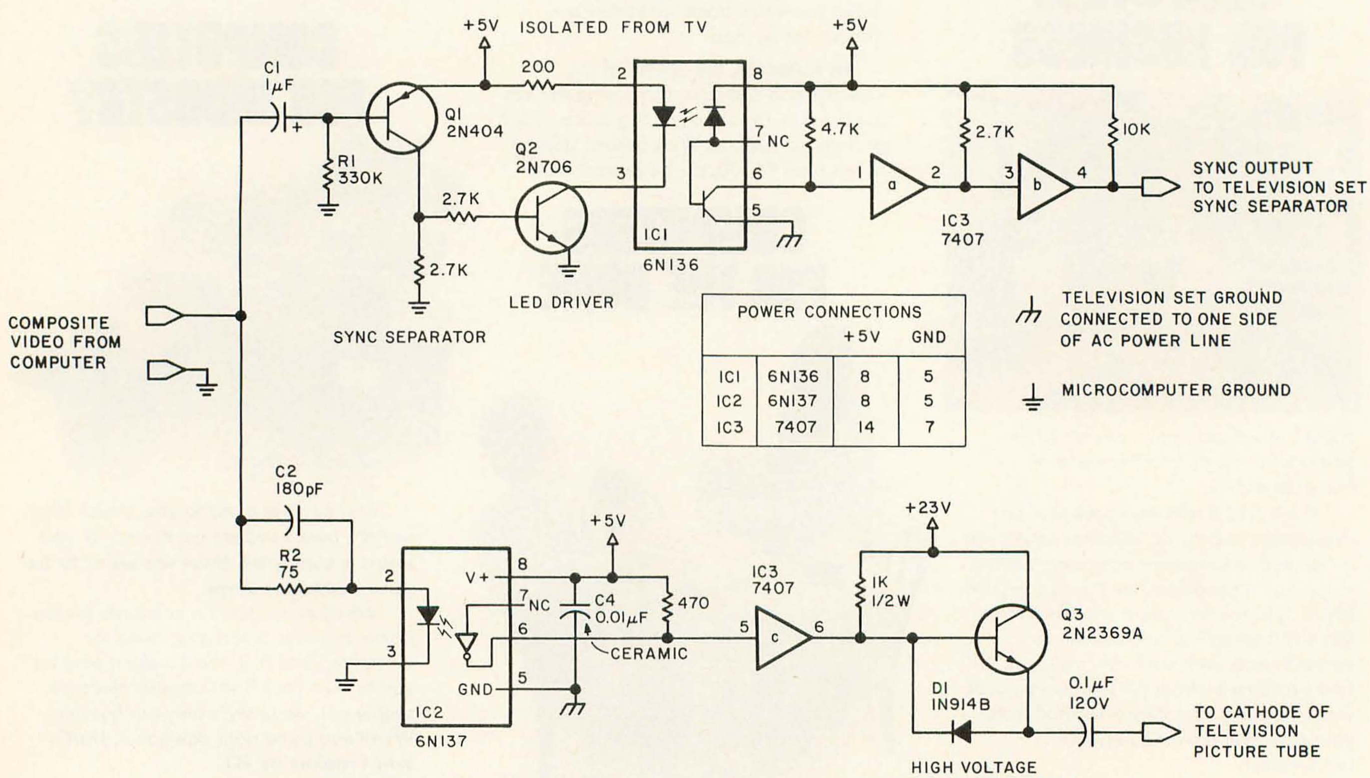


Figure 1: Schematic diagram for the microcomputer-to-television interface isolation circuit. Two different ground symbols are used to denote the isolation of ground paths. To maintain isolation, and therefore safety, the microprocessor should not be connected to any part of the television set. Integrated circuit IC3 is an open collector, high voltage, hex buffer of type 7407. Capacitor C4 is a 0.01 µF ceramic type used for bypass. The +5 V supply for the sync separator and LED driver is taken here from the video output jack of the TRS-80. It should come from the computer's power supply if used with another computer.

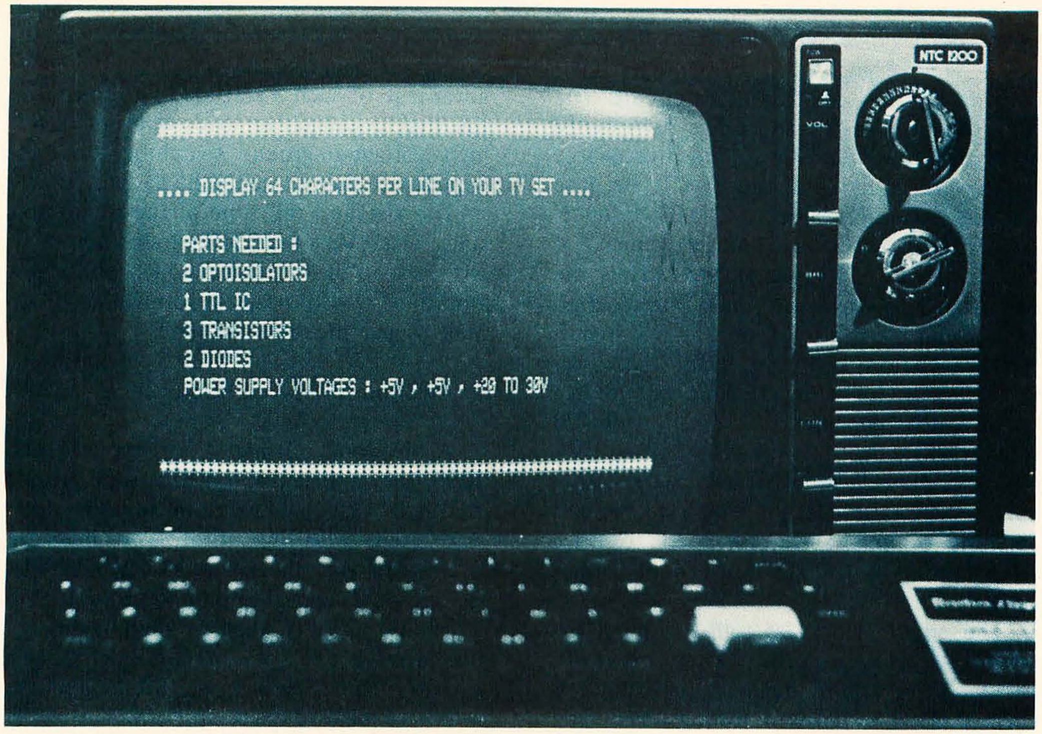


Photo 1: An example of the high quality display produced by using the circuit described here with a Radio Shack TRS-80 microcomputer and NTC 1200 television set.

Among the factors making extension of bandwidth difficult are the Miller effect (which says that the effective base-to-emitter capacitance of a transistor is increased because of the added induced charge due to the collector-to-base capacitance), transistor gain bandwidth limitations, stray wiring capacitance, and picture tube capacitance. Even if you somehow manage to make your set display 64 or more characters per line, you probably will not be able to use it as a regular television receiver any longer.

A More Direct Approach

When I ordered a TRS-80 microcomputer from Radio Shack I decided not to buy the matching video monitor. Instead I bought a television set in order to convert it for use as a video monitor. My goal was to obtain the 5.5 MHz bandwidth required for the TRS-80.

At first I tried redesigning the video amplifier of my new set. However, I soon discovered the difficulty of designing an amplifier with the necessary bandwidth and the gain necessary to drive the set's cathode ray picture tube.

Fortunately, after considerable experimentation, I came up with a solution to the problem. The answer was to bypass the set's video amplifier circuitry and drive the picture tube directly with a digital circuit. This is the easy way to get the bandwidth needed. Since the picture tube is primarily a capacitive load, the digital circuit must be carefully designed to handle it.

The Digital Driver Circuit

A schematic of the interface circuit is given in figure 1. This circuit was designed for use with TRS-80, but it should work for any system with a standard composite video signal output. The composite video signal is separated by the circuit into its video and sync components. Each digital signal is separately transmitted through optoisolators. The received portion of video signal is buffered and goes to the high voltage driver stage, which is connected to the television set's picture tube. The sync portion is buffered and goes to the sync separator of the set.

Circuit Description

The optoisolators, two integrated circuits shown in the schematic as IC1 and IC2, electrically isolate the microprocessor from the television set. On one side of the optoisolator is an LED (light emitting diode) which emits photons that the other side of the device receives with a photodiode. IC1 has an internal transistor to amplify the photodiode signal; IC2 has an internal integrated amplifier. The incoming composite video signal has a white level of +2 V, black level of 0.5 V and a sync level of zero volts. The LED in IC2 responds only to the video portion of the signal, since it requires 1.5 V to turn on. C2 is a speed-up capacitor.

The sync separator made up of capacitor C1, resistor R1, and transistor Q1 effectively

slices the negative sync tips from the composite video signal. The base emitter junction of Q1 acts as a detector circuit. The time constant of R1 and C1 is sufficiently great to allow a substantial positive charge buildup on the right side of C1. Because of this, Q1 is reverse biased and conducts only during the negative going sync peaks of the composite video signal. Q2 buffers the sync signal to drive the LED. The received sync signal on the right side of IC1 is buffered by sections IC3A and IC3B.

IC2 is a high speed, TTL compatible optoisolator capable of transmitting 20 million bits per second. IC3C, transistor Q3, and diode D1 make up a high voltage totem pole output stage. Integrated circuit versions of this stage are used to drive loads of up to 1000 pF at switching rates of up to 2 MHz.

The circuit works as follows: when the output of IC3C goes low, Q3 is turned off. Load current from the load capacitance is then shorted to ground through the open collector output transistor of IC3C. When it goes high, Q3 is turned on and the current is sourced from the +23 V supply. The major advantage of such a stage is that it can drive the highly capacitive loads without having high voltage-to-ground switching transients common in many totem pole designs.

The rise and fall time of the totem pole stage was measured to be less than 15 ns with a load of 40 pF. An equivalent analog amplifier would need a bandwidth of 23 MHz to give the same rise time.

Connection to the Television Set

A National Trade Corp model NTC 1200 set (a black and white type with a 12 inch diagonal measure picture tube) was used with the prototype interface circuit. It was the cheapest 12 inch television set I could find that came with a schematic. I was able to obtain this set for around $80. It's almost identical in circuitry to a Sharp model 3K-73 and I'm sure it's similar to many others.

A simplified schematic of the video

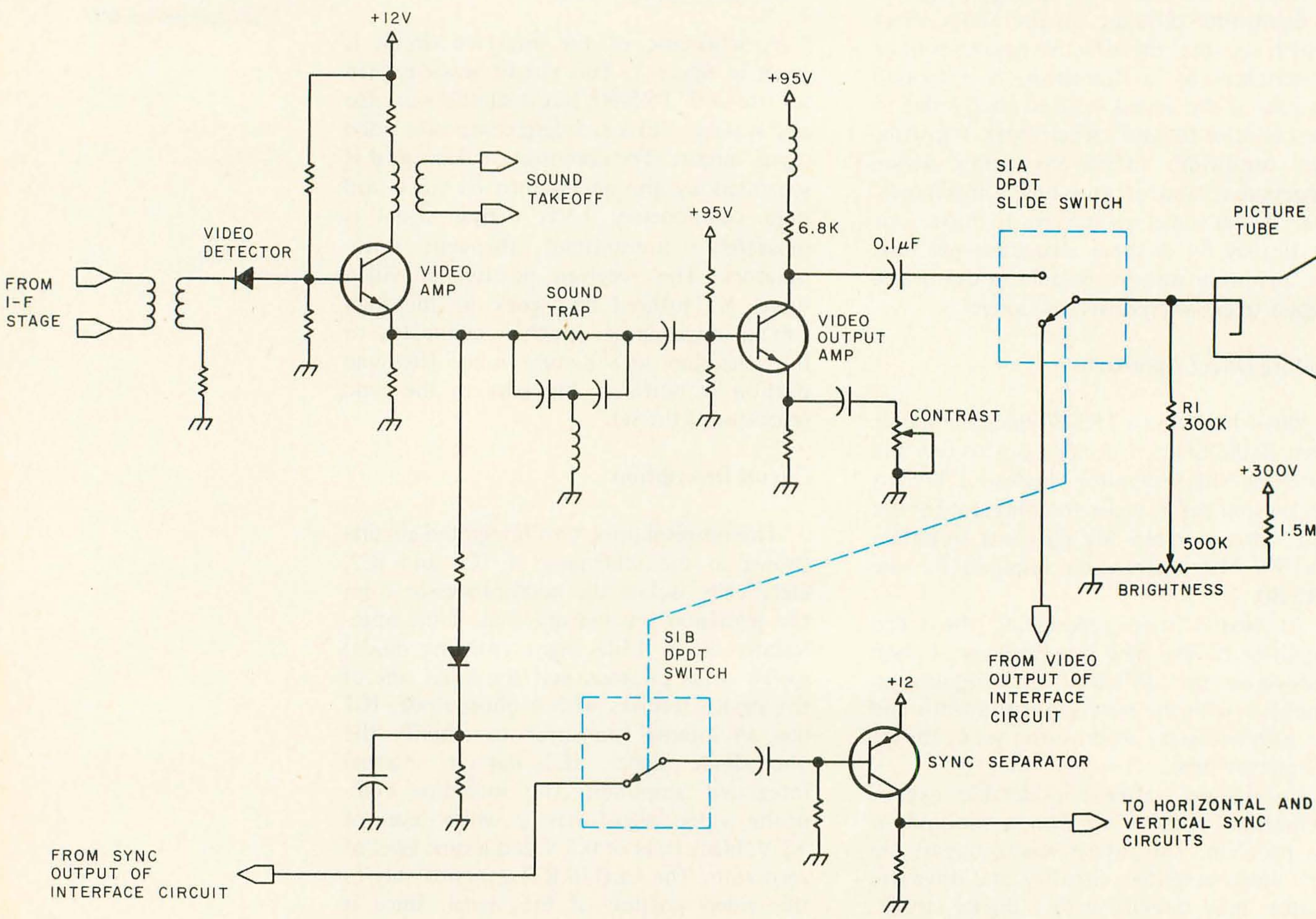


Figure 2: Simplified schematic diagram of the video output stage of the NTC 1200 television. This is typical of recently manufactured inexpensive sets. The DPDT (double pole-double throw) slide switch enables selection of function as television receiver or as video monitor.

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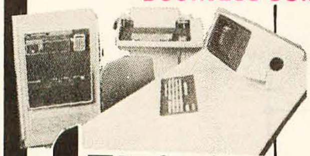


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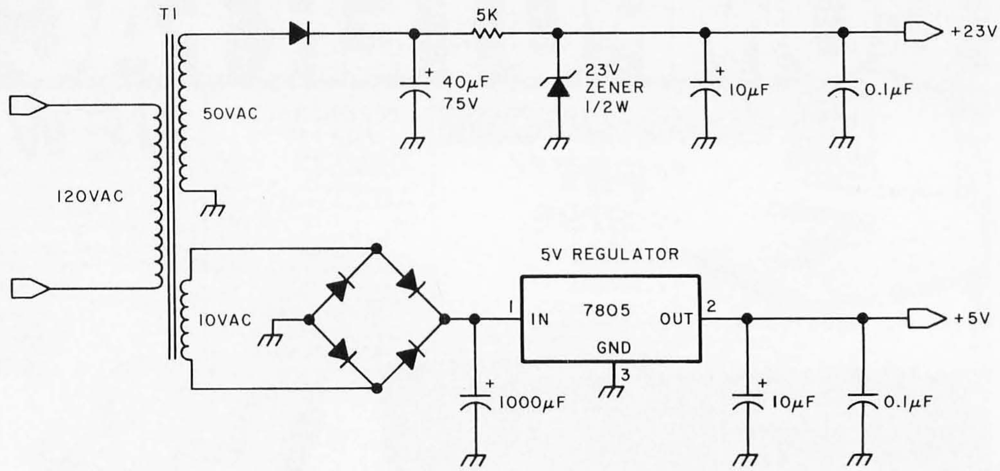


Figure 3: Schematic diagram of the power supply for the set side of the interface and for the driver circuit. Transformer T1 is a JE-100 type available from Jameco Electronics. The primary is 120 VAC; the secondaries provide 10 VAC at 50 mA and 50 VAC at 30 mA. The rectifier diodes should have appropriate current ratings.

output stages of the set and the points where the interface circuit is connected is shown in figure 2. The video amplifier output is normally AC coupled to the cathode of the picture tube. This is a common practice in low cost portable TV sets. This is an advantage in that it also allows the interface circuit to be AC coupled and not affect the DC biasing of the picture tube, which controls the screen brightness.

The interface circuit sync signal output is fed into the television set's sync separator. Some sets modulate the grid with video instead of the cathode. In that case a 7406 hex inverting buffer should be used instead of the 7407 buffer to obtain the proper polarity. Any TV set may be used with the interface circuit. A newer, small screen set is preferred. If the 23 V signal isn't sufficient drive to give a good display on the screen, the power supply voltage may be increased to a maximum of 30 V, the breakdown voltage of IC3. DC restoration of the video signal at the cathode with a clamping diode will also help. A picture of the display obtained by using this system with my TRS-80 microcomputer is shown in photo 1.

Power Supply

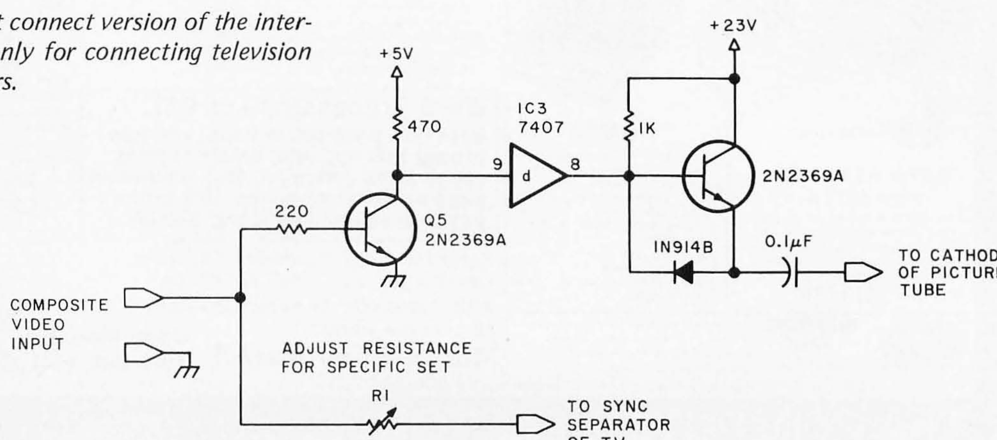
Figure 3 shows a schematic of the power supply used. It supplies +5 V at 40 mA for IC1, IC2 and IC3, and supplies +23 V at 5 mA for the high voltage output stage. If you are clever, you can use the television set's power supplies to get the +5 V and +23 V. But be careful: the cheaper solid state TV sets are designed to the limit. Drawing 40 mA for the +5 V supply might be an excessive load on the set's power supply.

The interface circuit also requires a +5 V at 5 mA isolated supply. This should come from the microprocessor. A TRS-80 has this voltage conveniently available at the video output jack.

Direct Connect Version

If you have a television containing its own power supply transformer isolating it from the AC power line, you can use a direct connect version of the circuit. A schematic of this version is shown in figure 4. Transistor Q5 responds only to the video

Figure 4: Schematic of the direct connect version of the interface circuit. This may be used only for connecting television sets containing power transformers.



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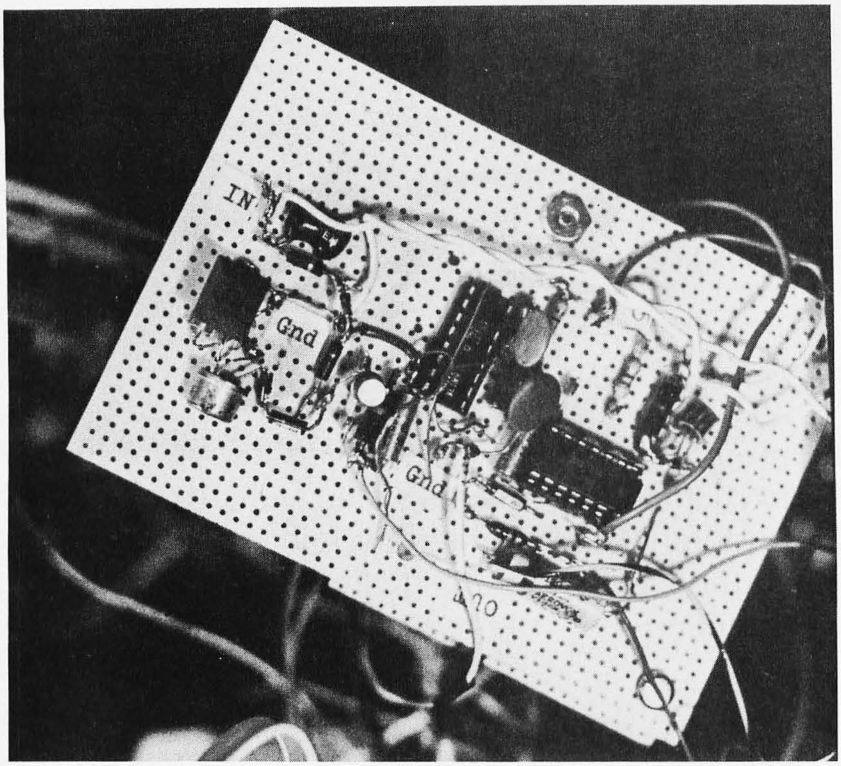


Photo 2: Closeup of the circuit as constructed on a piece of perforated project board. Layout of the components was conducted following guidelines set forth in the text.

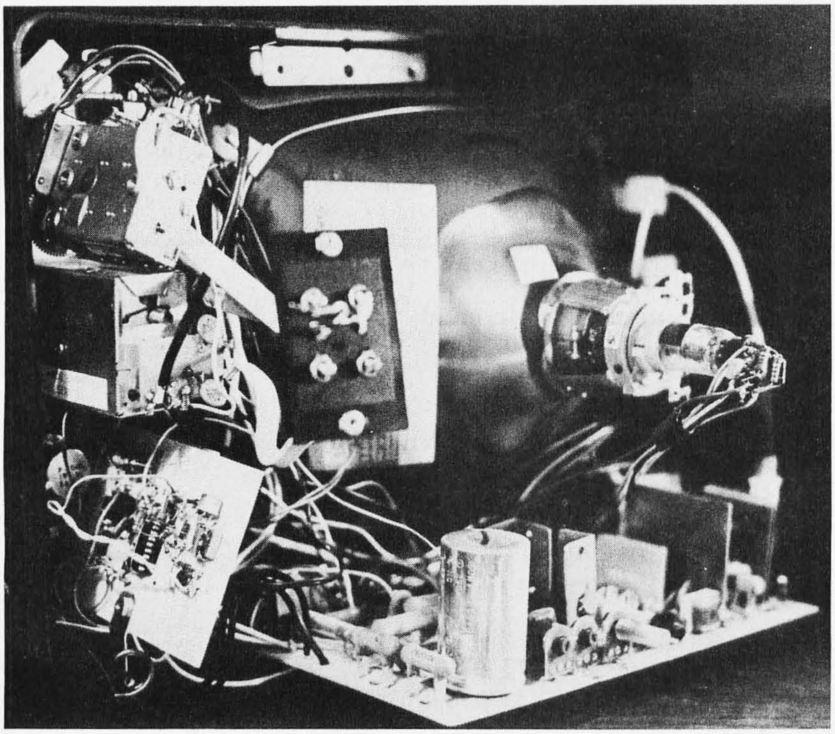


Photo 3: Interior of the television set with the computer interface circuit installed below the tuner. Great care should be taken when you work inside the television set, since high voltages are present while it operates. Television repair manuals are full of precautions which should be observed.

portion of the composite video signal. The composite video signal is fed through the resistor R1 directly to the television set's sync separator.

This version should be used only if the television set has its own power supply transformer. The optoisolators are used to prevent injury to people and damage to equipment that can occur from accidents and malfunctions involving circuits which are not isolated from the power line.

Circuit Layout

Proper circuit layout is important for proper circuit operation. The connection to the cathode of the picture tube *should* be as short as possible. This minimizes capacitive loading of the totem pole output stage, which would degrade the picture quality. The cathode connection should be kept away from the flyback transformer and the incoming 60 Hz line voltage.

The input optoisolator circuitry must be well separated from the output circuitry. Circuit wiring, especially that pertaining to the video signal, must be kept short. For high speed operation, pin 7 of both IC1 and IC2 should be clipped from the package. This ensures that the base to collector capacitance of IC1 and the input/output capacitance of IC2 is kept to a minimum.

A 0.01 μF ceramic capacitor should be connected directly to the pins of IC2 for good power supply decoupling. If you use a printed circuit board, run a ground trace midway between the pins of each optoisolator, connected to the output ground. If you use another method of construction, such as vector board, run a small piece of wire under the integrated circuits to act as a ground trace. This aids common mode signal rejction of the optoisolators.

Photo 2 shows a close view of the circuit as constructed on a section of perfboard. Photo 3 shows the circuit nestled into its operating position in a convenient space beneath the set's tuner.

Getting the Bugs Out

If, after you build the circuit, the characters on the display are not sharp and clear, the interface circuit does not have enough bandwidth. The first thing to do is to disconnect switch S1 and wire the output of the interface circuit directly to the cathode ray tube. The current limiting resistor (R1 in figure 2) should be taken off the television set's circuit board and mounted

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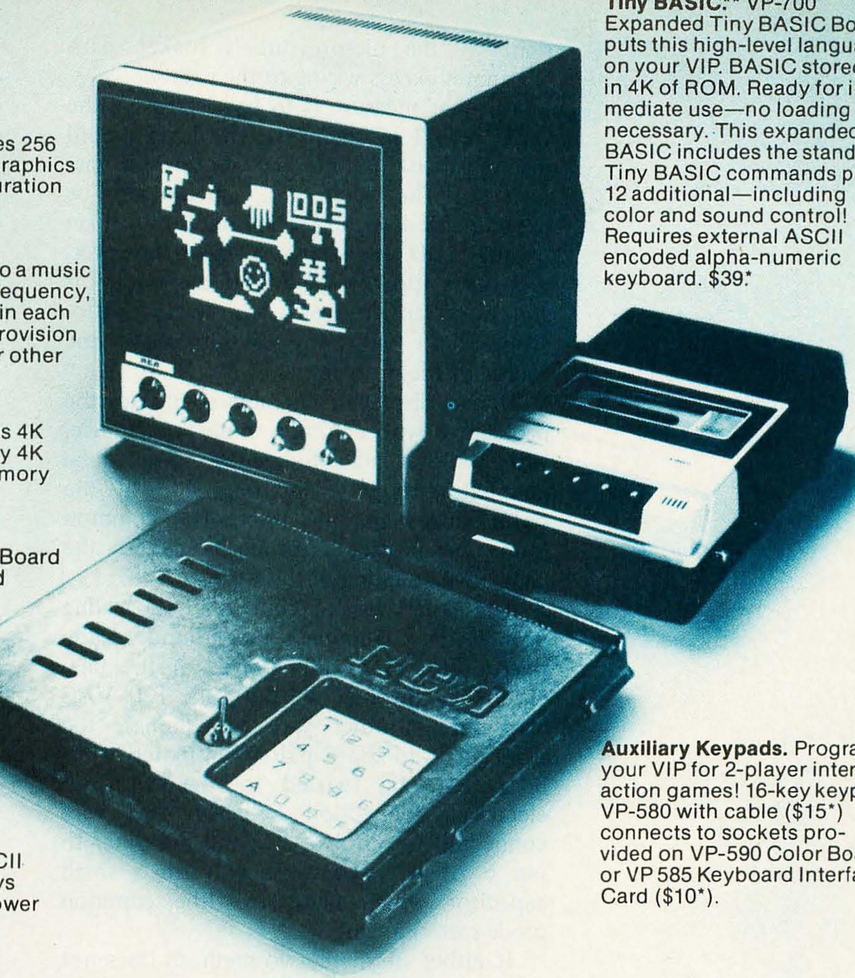
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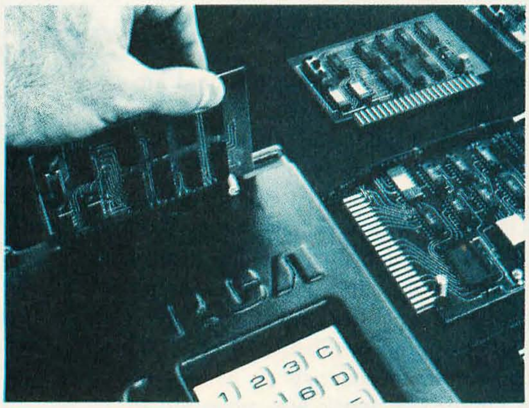
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right at the picture tube's socket. This eliminates excess wiring to the cathode.

Another measure is to try decreasing the value of R2 in figure 1. The LED should receive about 15 mA of current for fast turn on. The value of C2 should also be experimented with. C2 speeds up turn on of the LED. Too large a value, however, will cause turn off delays. If the display is still not sharp, use of a wide band oscilloscope is the only way to track down the source of the problem.

If the displayed characters sparkle, the problem is with common mode capacitance, which allows high frequency noise to be coupled through from one side of the optoisolators to the other. The common mode capacitance is primarily due to the capacitive coupling of the wiring.

The easiest way to eliminate the sparkling problem is to connect the ground of the microprocessor to the ground of the television set through a 1000 pF, 120 VAC capacitor. Another way to eliminate the problem is to use a pair of insulated wires 3 inches long twisted together with no electrical connection between, one wire connected to pin 3 of IC2 and the other to pin 6 of IC2. These wires form a small capacitor which neutralizes the common mode capacitance.

If either of these two methods does not solve the problem, the chances are that you have poor circuit board layout and you should rewire your circuit board, making sure that your input optoisolator circuitry is well separated from the television set's circuitry, especially from the flyback and the AC line voltage. In the same manner, keep the connections to the picture tube away from the other circuitry.

Displaying More Than 64 Characters per Line

The TRS-80 displays 64 characters per horizontal scan line in only 36 μs. If it were redesigned, it could display 80 characters per line in 45 μs without changing its pixel rate, and still fit them on the video display screen. Therefore, the interface circuit should probably work for any system which displays 80 characters per line.

The maximum frequency at which the interface circuit can work was measured to be 8 MHz. The major limitation to the display rate is the delay time of the circuit. The delay time is the interval it takes the circuit output to begin to respond to the input signal. The delay time of the circuit was measured to be 55 ns, whereas the rise and fall times are only 15 ns. About half of the delay is due to the optoisolator and the other half occurs in the totem pole output stage.

For high resolution graphics, another driver stage design must be used. One possibility is the use of the newer, high speed Schottky MOS clock drivers with on/off times of about 15 ns. The optoisolators may not be used because of their limited frequency capabilities.

A good example of a high resolution cathode ray tube driver is the design used in the Hewlett-Packard Model 9845A desktop computer. (See reference 6 for the hardware description.) It displays using a video clock rate of 21 MHz. One of the interesting points of its design is the use of a compensation inductor added in series with the cathode of the display tube. It provides approximately 7% overshoot of the cathode voltage in response to a step input, speeding up turn on of the display tube.

Before You Start. . .

Before you start working on your television set, you should have a schematic diagram of its circuit. A copy of Don Lancaster's *TV Typewriter Cookbook,* (Howard W Sams and Company Inc, Indianapolis, 1976), a classic in the field of TV displays, is also useful. It will help you figure out where and how to hook the interface circuit to your set. And don't overlook books on television set theory available at your local library. They are a gold mine of information and they will help you unravel the mystery of your set.

If you have difficulty finding a schematic of your set locally, the Howard W Sams Company has data for many sets in its *Photofact* series. Its address is 4300 W 62nd St, Indianapolis IN 46268.■

REFERENCES AND SUGGESTED READING

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2. *National MOS Integrated Circuit Databook, 1974 edition* (section on MOS clock drivers) National Semiconductor Corp, 2900G Semiconductor Dr, Santa Clara CA 95051.
3. *Hewlett-Packard Application Note 947,* "Digital Data Transmission Using Optically Coupled Isolators," Hewlett-Packard Corp, Palo Alto CA 94304.
4. *Hewlett-Packard Application Note 939,* "High Speed Optically Coupled Isolators," as above.
5. Hewlett-Packard Optoelectronics Staff, *Optoelectronics Applications Manual,* McGraw-Hill, New York, 1976.
6. *Hewlett-Packard Journal,* April 1978, pages 16 thru 18, Model 9845A desktop computer hardware design description, high resolution video display.

Book Reviews

Computers in Laboratory Medicine
edited by Derek Enlander MD
Academic Press, New York
$14

As a student of medical applications of computers I have found relatively few books written about the up to date use of computers in medicine; and those one does find are usually reviews of commercially available systems. It is refreshing to find that the book *Computers in Laboratory Medicine*, edited by Derek Enlander MD, is a forward looking work in which the uses of microcomputers are considered in various clinical laboratory applications.

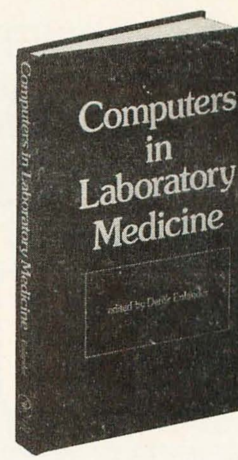
The book is concise and well-designed. The various chapters are written by a veritable who's who in clinical computerization. George Z Williams MD, who retired as head of clinical laboratories at the National Institutes of Health, has written the initial chapter in a philosophical tone, quoting aspirations of Buckminister Fuller. He points the way forward for the next chapter in which the editor, Enlander, writes of his personal experience in developing a discrete front end processing system. The initial development took place at Stanford University Medical Center in 1968. While this was obviously before the advent of microprocessor chips, the spark of ingenuity had been kindled. The following chapter contains a description of another preprocessing approach using Hewlett-Packard desk top calculators as the preprocessing modules. In a third section Dr Blois of the University of California elegantly ties the front end lab systems into a hospital-wide system.

A medical diagnosis technique called anatomic pathology is often a forgotten orphan when computerization of pathology is discussed. It does not have the glamour of real time data acquisition, but is nevertheless an important problem of data manipulation and retreival. Two experts on this subject are Dr Pratt and Dr Lamson; each provides a chapter on his experiences in this field.

Nuclear medicine is looked at from two facets, static and dynamic imaging, followed with a chapter by Dr Budinger, an electrical engineering PhD as well as an MD, who delves into the tomorrow world of three-dimensional imaging by way of radioisotopes. The development of the mathematical models and Fourier transforms are covered in depth. Dr Weber discusses and reviews the time-function studies in organ imaging.

This book is closed in a fitting manner by Dr David Seligson of Yale who points to the vast future need of modular processing of medical laboratory data. He emphasises the previous authors' ideas on the use of microcomputers in medicine.

If one was to fault the book it would be on its price of $14, its seemingly short supply, and the long delay on ordering. I must thank Seaton's, 26 O'Farrell St, San Francisco, for their help in supplying the book, even when the publishers could not.



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Life versus Computer Capacity

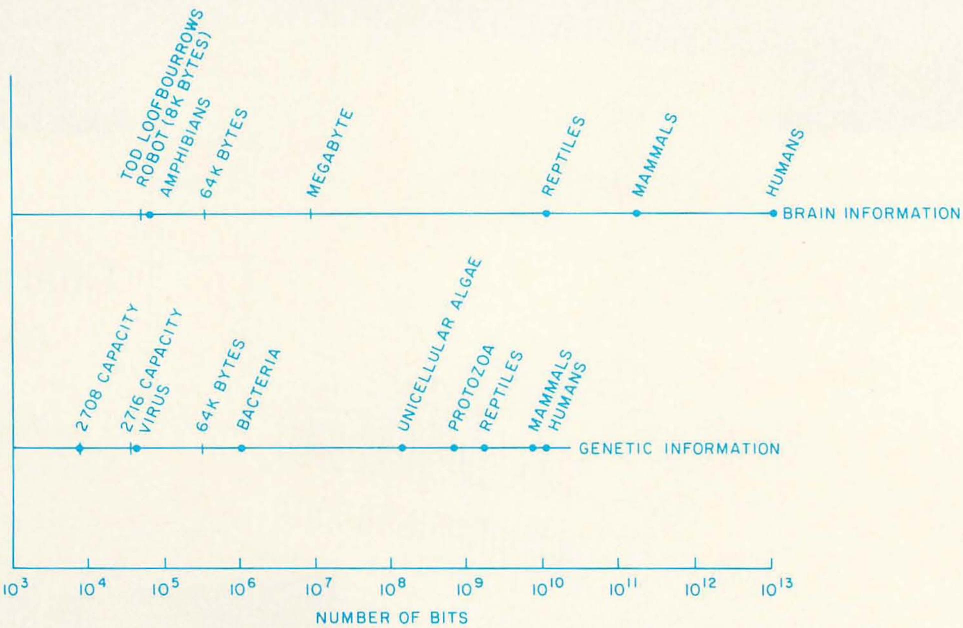


Table 1: Information content comparison adapted from Carl Sagan's The Dragons of Eden, *which was derived from Britten and Davidson, "Gene Regulation for Higher Cells: A Theory,"* Science, *July 25 1969, pages 349 thru 357. The brain information is considered to be programmable memory. The genetic information is derived from the number of deoxyribonucleic acid (DNA) per haploid cell. It is considered to be the read only memory comparison figure.*

Patrick H Stakem
42F Ridge Rd
Greenbelt MD 20770

I have taken the chart of the evolution of information on page 26 of Carl Sagan's book, *The Dragons of Eden,* and extracted the number of bits of read only memory and programmable memory for different taxia. I then added some items familiar to most computer experimenters, such as the 2708 and 2716 read only memories, a 1 megabyte marker, and the on board capacity of Tod Loofbourrow's robot (8 K bytes, I believe). The result is table 1.

Information in the DNA nucleotide pairs is a type of read only memory expressable in bits. Sagan's chart is derived from "Gene Regulation for Higher Cells: A Theory," by Britten and Davidson, *Science,* July 25 1969, pages 349 thru 357. One caveat: comparing the estimates of the amount of information in the brain (whatever that is) to an amount of random access memory is misleading. There is no clear knowledge that the brain is arranged anything like a digital system. Also, I have ignored information processing capacity and rate and merely compared storage of information.

Making allowances for different implementations, if we work from a functional specification for, say, a dog, do we need to include 10^{11} bits of programmable memory and 5×10^9 bits of read only memory in the robotic version?

We may be in a period of *robotic evolution* as we see digitally implemented mobile systems becoming more sophisticated and prices coming down: it is now possible to own a 64 K byte home computer system without mortgaging the home.

I believe that such robots will have to be much more sophisticated than they are now before we're satisfied. On the other hand, the capabilities of Tod's robot or Allen and Rossetti's light-seeking Tee Toddler is more than one would guess from the memory capacity alone.■

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2. Loofbourrow, Tod, *How to Build a Computer-Controlled Robot,* Hayden Book Company Inc, Rochelle Park NJ, 1978.

3. Sagan, Carl, *The Dragons of Eden: Speculations on the Evolution of Human Intelligence,* Random House, New York, 1977.

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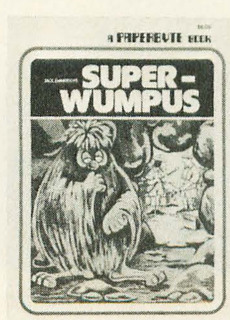
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The author, Paul Warme, has also included a BASEX Loader program which is capable of relocating programs anywhere in memory.

NEW

ISBN 0-931718-05-8
Author: Paul Warme
Pages: 88
Price: **$8.00**

PROGRAMMING TECHNIQUES is a series of **BYTE BOOKS** concerned with the art and science of computer programming. It is a collection of the best articles from BYTE magazine and new material collected just for this series. Each volume of the series provides the personal computer user with background information to write and maintain programs effectively.



The first volume in the Programming Techniques series is entitled **PROGRAM DESIGN.** It discusses in detail the theory of program design. The purpose of the book is to provide the personal computer user with the techniques needed to design efficient, effective, maintainable programs. Included is information concerning structured program design, modular programming techniques, program logic design, and examples of some of the more common traps the casual as well as the experienced programmer may fall into. In addition, details on various aspects of the actual program functions, such as hashed tables and binary tree processing, are included.

ISBN 0-931718-12-0
Editor: Blaise W. Liffick
Pages: 96
Price: **$6.00**

SIMULATION is the second volume in the Programming Techniques series. The chapters deal with various aspects of specific types of simulation. Both theoretical and practical applications are included. Particularly stressed is simulation of motion, including wave motion and flying objects. The realm of artificial intelligence is explored, along with simulating robot motion with the microcomputer. Finally, tips on how to simulate electronic circuits on the computer are detailed.

ISBN 0-931718-13-9
Editor: Blaise W. Liffick
Pages: approx. 80
Price: **$6.00**
Publication: Winter 1979

RA6800ML: AN M6800 RELOCATABLE MACRO ASSEMBLER is a two pass assembler for the Motorola 6800 microprocessor. It is designed to run on a minimum system of 16 K bytes of memory, a system console (such as a Teletype terminal), a system monitor (such as Motorola MIKBUG read only memory program or the ICOM Floppy Disk Operating System), and some form of mass file storage (dual cassette recorders or a floppy disk).

The Assembler can produce a program listing, a sorted Symbol Table listing and relocatable object code. The object code is loaded and linked with other assembled modules using the **Linking Loader LINK68.** (Refer to **PAPERBYTE™** publication **LINK68: AN M6800 LINKING LOADER** for details.)

There is a complete description of the 6800 Assembly language and its components, including outlines of the instruction and address formats, pseudo instructions and macro facilities. Each major routine of the Assembler is described in detail, complete with flow charts and a cross reference showing all calling and called-by routines, pointers, flags, and temporary variables.

In addition, details on interfacing and using the Assembler, error messages generated by the Assembler, the Assembler and sample IO driver source code listings, and **PAPERBYTE™** bar code representation of the Assembler's relocatable object file are all included.

This book provides the necessary background for coding programs in the 6800 assembly language, and for understanding the innermost operations of the Assembler.

ISBN 0-931718-10-4
Author: Jack E. Hemenway
Pages: 184
Price: **$25.00**

to order books see next page . . . . .

BYTE News....

ATARI'S NEW COMPUTERS. The recently announced Atari Model 400 and 800 personal computers are major entries into the market. The 8 K nonexpandable 400 (suggested retail $500) sports a touch audio feedback keyboard and a single read only memory cartridge slot, plus cassette I/O. It also has 16 color graphics with eight luminance levels (!) The 48 K expandable 800 (suggested retail $1000 with 8 K and cassette recorder) has additional color features, full keyboard, 8 K BASIC, high resolution graphics, two read only memory cartridge slots, and much more. Both units use a modified 6502. Availability: August 1979 (limited quantities); full availability: Fall 1979. More details next month.

TI'S NEW PERSONAL COMPUTER. Rumors are flying about Texas Instruments' impending entry into the personal computing market. The unit will reportedly use the TMS 9900 processor with 40 K of read only memory circuits, will generate 20 lines of 40 characters on a standard television, will have provisions for accommodating video disk players and video tape recorders, and will have sophisticated sound production. Sources predict a mid-1979 unveiling.

TI AND GTE DEVELOPING HOME DATA RETRIEVAL SYSTEMS. Since Labor Day, Texas Instruments has been testing a "Teletext" home information system which displays on a standard home television set via a decoder unit. The decoder can be internal or external to the television set. It is expected that the decoder should add about $50 to the television's cost. The data is transmitted during the frame blanking time. The viewer can elect to view the data, the standard picture, or the data superimposed on the picture. Testing should continue throughout 1979. FCC approval is required.

Last October General Telephone & Electronics gave a presentation and demonstration to the FCC of their system, which uses a microprocessor. It would allow a user to retrieve data from a number of different data banks and have it appear on their television screen. The system is still in a very early stage of development.

A television based data retrieval system, called Viewdata, is already in operation in Great Britain. It was developed by the British Post Office.

WORD PROCESSING PRINTERS USING DOT MATRIX ARE COMING. All present word processing printers use character impact printing mechanisms and are expensive (typically over $2000). The most popular are the Selectric, Diablo and Qume printers. Dot matrix printers are faster and cheaper but produce crudely formed characters generally considered undesirable for word processing applications. However, several companies are working on dot matrix printers to improve their printing quality. By moving the dots closer together to 1000 dots per inch or closer, characters can be formed which are very close to those of the Selectric. Further, since the dot matrix is under direct processor control, changing a character font requires only a program change rather than a type element change. Imagine being able to change from standard to italic type faces using only software! Although the initial entries (from RC Sanders Technology Systems Inc) in this area will cost more than present impact units, costs should decrease substantially to well below present units.

8080/8085 MICROPROCESSOR PRICES DROP. The 8085, Intel's 1 chip version of the 8080 with added features is now selling for $10 in OEM (original equipment manufacturer) quantities. The 8080 is now down in the $4 to $5 range. Actually the 8085 is in effect cheaper than the 8080 since it does not need extra support devices and works off only 5 VDC. Therefore, most of the new 8080 designs now use the 8085. It is expected that the 8085 will be down in the $4 to $5 range by year's end. The importance of this is that the microprocessor is now insignificant in cost compared to memory and peripheral circuits.

WILL 16 BIT PROCESSORS TAKE OVER? Not yet, at least. There is reason to question whether or not 16 bit processors have achieved the success in the personal computer marketplace achieved by the 8 bit machines. The fact is that there have been at least three 16 bit mainframes available in the personal computer marketplace for over a year now, namely the Technico 9900 computer, the Alpha-Micro computer, and the Heath H-11 computer. Although all three provide better performance than the 8 bit machines, their acceptance does not compare to the smaller machines. It will be interesting to see if any 16 bit mainframes using the Intel 8086 processor will be forthcoming in the near future.

16 BIT PROCESSORS TO BE SECOND-SOURCED. Intel has entered into an agreement with National Semiconductor for the latter to also manufacture the 8086, Intel's 16 bit processor. Zilog has also arranged for second sourcing of their new Z-8000 16 bit processor, but does not expect to be in production until the middle of the year. Intel has been in production on the 8086 since May of last year.

MICROCOMPUTER STANDARDS ARE FINALLY COMING. After several years of manufacturers going their own way in hardware and software design and causing numerous problems for users trying to interface components, the IEEE (Institute of Electrical and Electronic Engineers), the most powerful electrical engineering organization, is working to cure the problem. They expect to soon issue their first standard, which will standardize the S-100 bus. This should eliminate the problem of those S-100 compatible boards which do not work in many S-100 mainframes, (as so many S-100 system users learned the hard way). The fact that a board plugs into an S-100 bus does not guarantee that it will work. Now users can look for the statement "meets IEEE S-100 standards" to insure compatibility.

Standards are also being developed for relocatable loaders, mnemonic standards (particularly between the 8080 and Z-80), a floating point math standard for use with hardware floating point integrated circuits, Intel SBC bus and the National Micro bus standards (which will enable 6800 peripheral devices to work easily with 8080 and Z-80 integrated circuits). It is expected that the floating point standard will be appearing next after the S-100 standard.

PASCAL PICKS UP STEAM. The Pascal language is now the second most popular microcomputer high level language, second only to BASIC. Versions are already available for systems using the following processors: 8080, Z-80, 9900 and LSI-11. Soon two more will be added to the list: the 6502 (for Apple II systems) and a Western Digital chip set which executes Pascal machine code directly.

The popularity of Pascal is due to the fact that the language allows very concise expression of algorithms and is easy to use. It is block structured, has extensive data types and good control structures, providing nonverbose, easily understandable code. However, a large memory and a large disk system is required. Further, the versions currently available still lack certain features, which in time, I am sure, will be implemented. Pascal is considered a real programmer's language, whereas BASIC is considered by many to be a beginner's language.

Credit for the increasing popularity of Pascal goes to Dr Ken Bowles at the University of California–San Diego, who, with his students, has written several Pascal versions and is coordinating and standardizing the different available versions to increase software portability from system to system.

WHAT WILL HAPPEN TO MEMORIES IN 1979? This past year saw dramatic improvements in semiconductor memories that permitted large memory systems at low cost in microcomputer systems. There are already a great many home systems with 65 K of memory, and some with more. The significant areas of improvement are:

SEQUENTIAL MEMORIES: Look for ready availability of 256 K CCD (charged-coupled device) and bubble memories. 1 M byte versions will not be available until 1980. Costs will still be significantly greater than disks. This means that these devices will be used mainly for buffer applications and will not impact the disk storage area.

PROGRAMMABLE MEMORIES: They will be faster, cheaper, and more dense. 16 K dynamic programmable memories organized as 16 K by 1 bit and 2 K by 8 bit will be available that can operate on a single 5 VDC power supply. Also, look for refresh circuitry to be external to the memory devices.

ERASABLE READ ONLY MEMORIES: This year will see the availability of the 32 K erasable read only memory, organized as 4 K by 8 bits. A circuit will be introduced which combines a 1 K programmable memory and a 1 K read only memory. On power up, the program from the read only memory is loaded into the programmable memory. However, if the power fails, the program is retained in the read only memory section and bootstraps itself back into the programmable memory when power is restored.

6502 PROCESSOR MOST POPULAR OF THEM ALL. The 6502 processor will soon be the most widely manufactured processor circuit. It is already being made by MOS Technology, Synertek and Rockwell. Now it will also be made by Electronic Memories & Magnetics, and negotiations are under way with General Instrument. According to the most recent sales reports there are more 6502 ICs being manufactured than any other processor, including the 8080 and Z-80. The 6502 is currently being used in the APPLE, PET, KIM and several other personal computer systems. However, most of the production goes to high volume dedicated game use.

VIDEO DISPLAY TERMINALS ARE CHANGING. More and more CRT terminal manufacturers are introducing terminals utilizing the new video display controller chips that operate in conjunction with a processor. The result is that the component count decreases and performance increases. The most popular video display terminal, up to now, has been the ADM-3A. This was the first video display terminal to break the $1000 barrier and currently sells at around $800. However, Hazeltine, Perkins-Elmer and others have recently introduced terminals having essentially the same features as the ADM-3A and selling for around $700 with the likelihood that they will soon sell in the $600 range. On the other hand, these companies have also introduced terminals with extended features beyond the ADM-3A, which sell in the $800 range. It is rumored that Lear Seigler will soon replace the ADM-3A, which is an all TTL design, with a microprocessor-controlled unit. LS has been known for their aggressive pricing practices in the past, and their new terminals could set new price and performance levels.

Sol Libes
ACGNJ
995 Chimney Rdg
Springfield NJ 07081

Continued from page 43

spec will not be met as that pin actually sources 2 mA into ground.

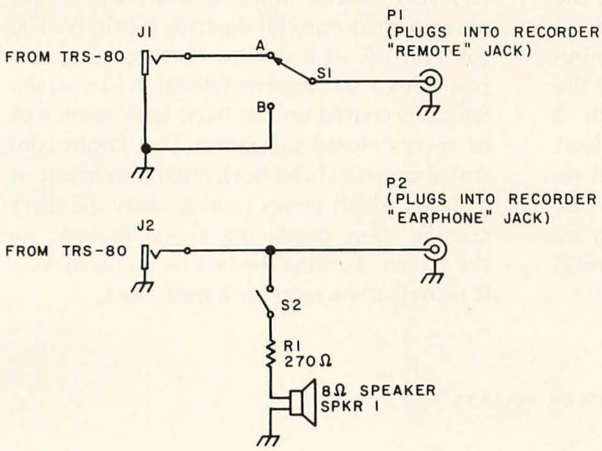
This means that although some 2708s may appear to program properly in the circuit shown, many may have weakly programmed bits, and over time the EPROM may appear to "drop" bits.

I would suggest using circuits recommended by Intel, as this will eliminate the possibility.

Jim Carlson
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Long Beach CA 90807■

Plugging a Jack in the Box

A graphics gremlin struck Craig Anderton's article in November 1978 BYTE ("A Cassette Interface Switching Box for the TRS-80," page 160). In figure 1, the schematic diagram, the symbols for jacks and plugs are reversed. The correctly drawn figure is shown here.■



Floating Point Error

In Burt Hashizume's article "Floating Point Arithmetic" (November 1977 BYTE, page 76) the statement was incorrectly made that the author was selling documentation for mathematical function software. Hashizume is selling the *program* and the documentation. The package includes arithmetic functions, square root, and transcendental functions written for the 8080 processor. The package may be obtained for $10 from the author at POB 447, Maynard MA 01754.■

A Big Memory?

On page 209 of the December 1978 BYTE our What's New? section introduced a 64 K byte programmable memory. Unfortunately, we said that the internal architecture was arranged as *64 K byte by 1*. We should have said it was 64 K words by 1 bit. Our apologies to all readers who thought that the age of the one memory chip computer had arrived.■

Another Plotter to Toy With

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Madison WI 53706

Technical Forum is a feature intended as an interactive dialog on the technology of personal computing. The subject matter is open-ended, and the intent is to foster discussion and communication among readers of BYTE. We ask that all correspondents supply their full names and addresses to be printed with their commentaries.

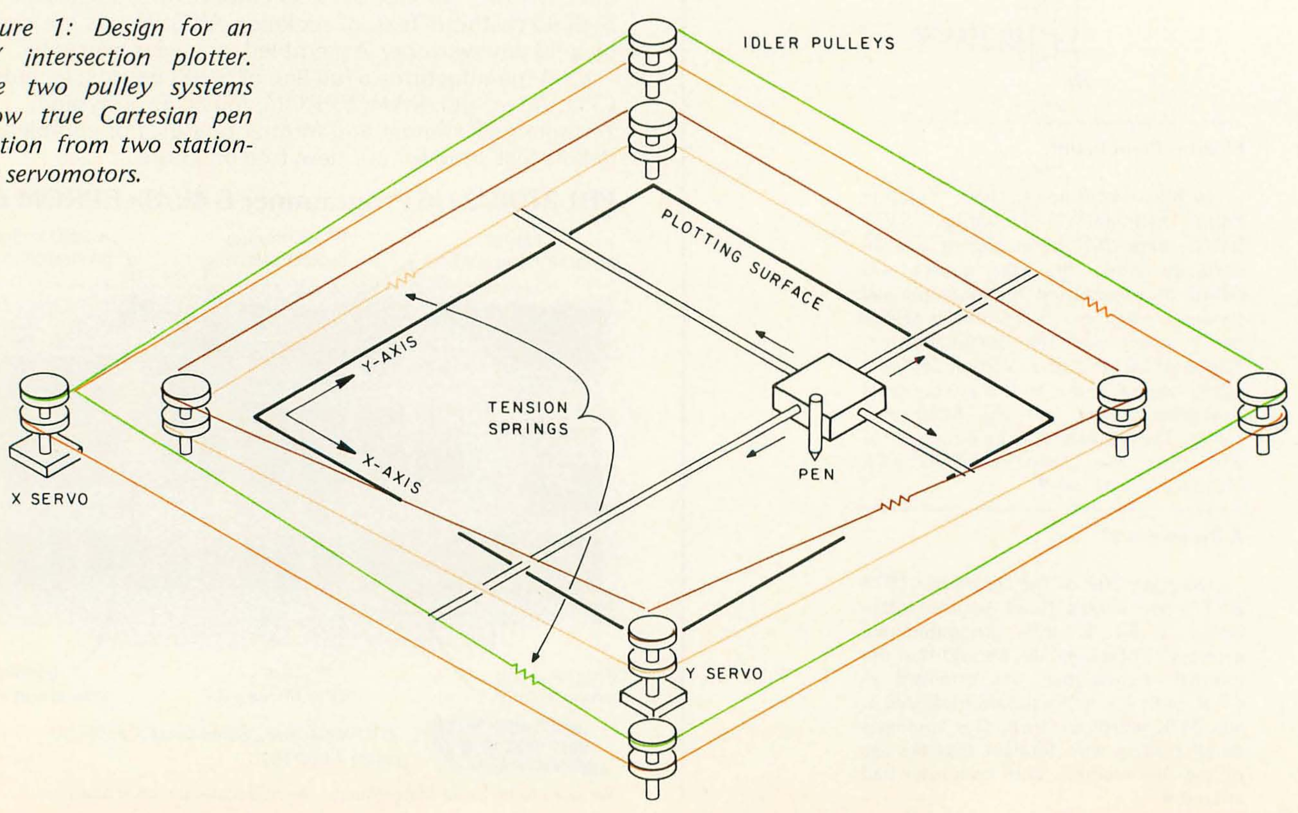
I have followed with interest past discussions of the possibility of building a hard copy pen plotter driven by hobby servomechanisms of the kind described by Robert Grappel in "Give Your Micro Some Muscles" (March 1977 BYTE, page 9).

The crux of the problem is finding an easy way to build mechanical arrangement for translating the rotary motion of a pair of servomechanisms into the two-dimensional translatory motion of a pen on a plotting surface. T P Roberts in "Some Plotting Comments" (February 1978 BYTE, page 172) has discussed this problem at some length. As pointed out in that article, a Cartesian XY plotting arrangement is by far the most desirable approach—both in terms of maximizing plotting accuracy and of minimizing software complexity. However, the design proposed by Roberts for such a plotter is, as he points out, rather difficult to execute. The main problem is that it requires one of the servomotors to be mounted on a moving platform driven by the other—a somewhat unstable mechanical situation.

I would like to point out, however, that an alternate design exists which solves this problem nicely. Moreover, a plotter employing this design has been available commercially for a good number of years. This device features high resolution, true XY plotting; it is ruggedly constructed, available off-the-shelf almost anywhere and sells for less than $10 (less the servomechanisms). This extraordinary product is manufactured by the Ohio Art company and, as any child could tell you, is sold under the name Etch-A-Sketch®!

No joke, this classic toy represents an excellent prototype for a hobbyist built plotter. Just in case there is anyone who has never owned one, I'll describe it briefly. The toy consists of a shallow rectangular plastic box with a transparent television-like screen which is coated on the back with some sort of silver colored substance. Two knobs control the vertical and horizontal movement of a stylus which serves to etch away the silver coating, thus producing a line drawing on the screen. Turning the box over and shaking it recoats the screen for a fresh start.

Figure 1: Design for an XY intersection plotter. The two pulley systems allow true Cartesian pen motion from two stationary servomotors.



Now, it's been a long time since I've had the tenacity to scrape clear the whole screen so as to see inside, but to the best of my recollection, the design of the toy is something like that shown in figure 1. Basically, it is an XY version of the intersection plotter described in the Roberts article. Lateral motion of the intersecting rods is accomplished by a system of pulleys and cords encircling the plotting area.

The trick is that each rod has two cords associated with it, threaded in opposite directions around the servomotor shaft pulleys. Thus, when the servomotor turns, the two cords move exactly the same distance around the plotting area, but in opposite directions, thereby keeping the rod parallel to its axis. Two such pairs of loops complete the system, comprising a simple, mechanically stable and quite satisfactory plotting mechanism.

Design Notes

Although figure 1 shows the drive pulleys mounted directly on the servomotor shafts, in practice it will usually be necessary to provide some sort of pulley or gear arrangement to adjust the amount of pen movement per revolution of the servomotor. When using servomechanism devices whose range is limited to 180°, an arrangement like that shown in figure 2 would be needed in order to obtain an adequate plotting area. If this is taken too far, of course, either the plot resolution will become unacceptably coarse, or else the torque at the secondary pulley will be reduced until it can no longer drive the mechanism smoothly.

A happier situation exists if one is working with devices (such as stepper motors) which can rotate continuously at a reasonable rate of speed. In this case, it is desirable to employ a reduction arrangement—just the opposite of that shown in figure 2. In this way, the size of the plotting area and the resolution can be increased.

A word also needs to be said about the pen mechanism. Any practical plotter requires the ability to raise and lower the pen under program control (the lack of this ability is a major shortcoming of the Etch-A-Sketch®). By far the simplest method is to employ gravity and the weight of the pen to maintain contact with the plotting surface (this works best with felt tip markers and Rapidograph type drafting pens). In this way, a very small solenoid is sufficient to lift the pen from the paper. Note that unlike Roberts' intersection plotter design, the pen need not be aligned with the intersection of the two drive rods: the orthogonal motion of the pen carriage insures that no distortions will be produced by an offset.

Two minor details also need mentioning. First, figure 1 shows the two sets of idler pulleys on different shafts only for clarity's sake; there's no reason why they can't all be mounted on the same shaft, provided that each rotates independently. Second, the illustration shows tension springs threaded in line with the drive cords. A generally better (but slightly more complex) method of maintaining tension is to spring load one of the idler pulleys for each loop as shown in figure 3. Note that the tension pulley for each loop must operate independently in order to compensate for small differences in the lengths of the cords.

Concluding Remarks

The design presented here possesses all the advantages of a true XY plotter com-

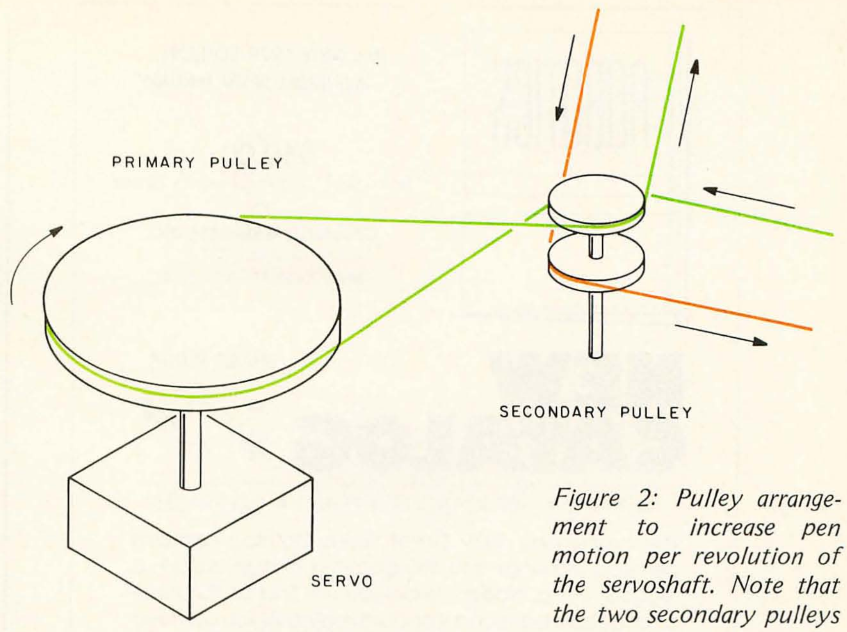


Figure 2: Pulley arrangement to increase pen motion per revolution of the servoshaft. Note that the two secondary pulleys must be attached together so that the servomotor will drive both cord loops, but in opposite directions. The arrows show the motion of the two loops for a clockwise rotation of the servomotor.

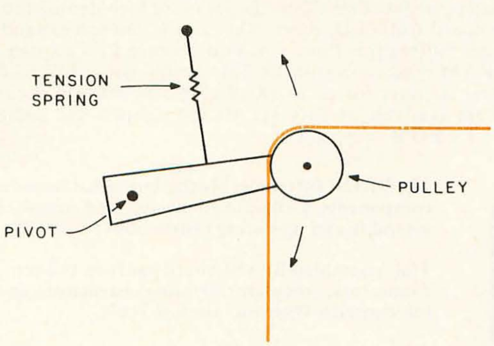


Figure 3: A spring loaded idler pulley to maintain cord tension. Four of them will be required, one for each loop.

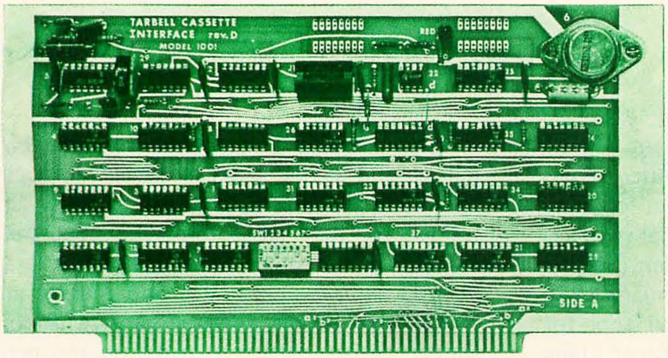
bined with an ease of construction that matches or exceeds most other designs which have been proposed. Carefully constructed and driven by appropriate software, it should be capable of producing plots of a quality approaching that of a professional draftsperson. A simple plotting routine might accept an X and Y coordinate relative to the current pen position (ie: delta X and delta Y) and either move (pen up) or draw (pen down) to that coordinate. A more elaborate plotting package might include routines for drawing dotted and dashed lines, automatic scaling, rotation, translation of the coordinate system, software character generation, etc.

Such a system would provide the basis for a variety of practical and aesthetic applications of personal computing. The artistic possibilities are especially appealing. Several BYTE covers have been graced with examples of "algorithmic art" (ie: February 1977, October 1977, April 1978, September 1978, etc). Given time, a pen plotter is capable of producing far more detailed and intricate images than can be satisfactorily displayed on a video display. An added bonus is the capability of making multiple passes with different colored pens.■

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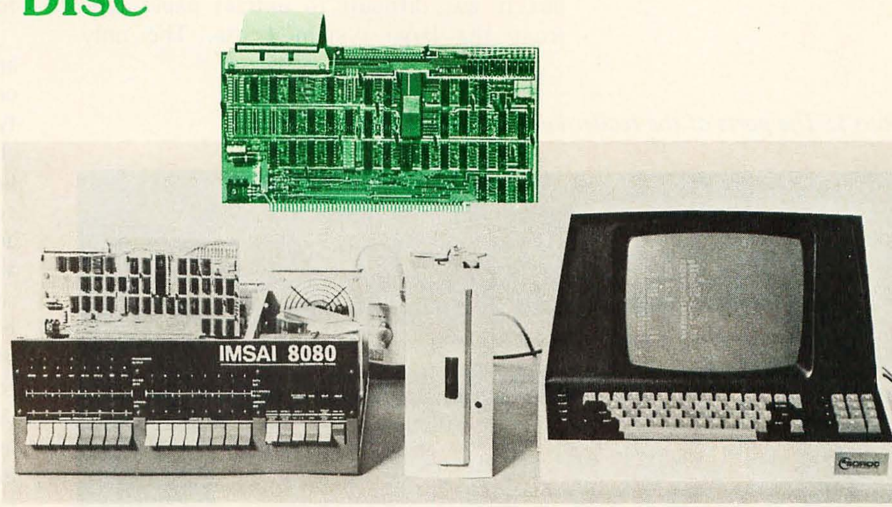


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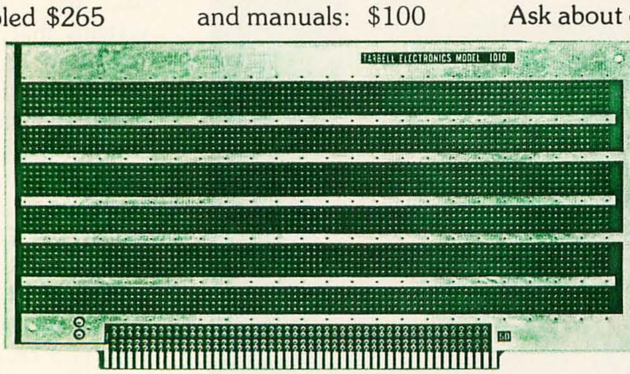
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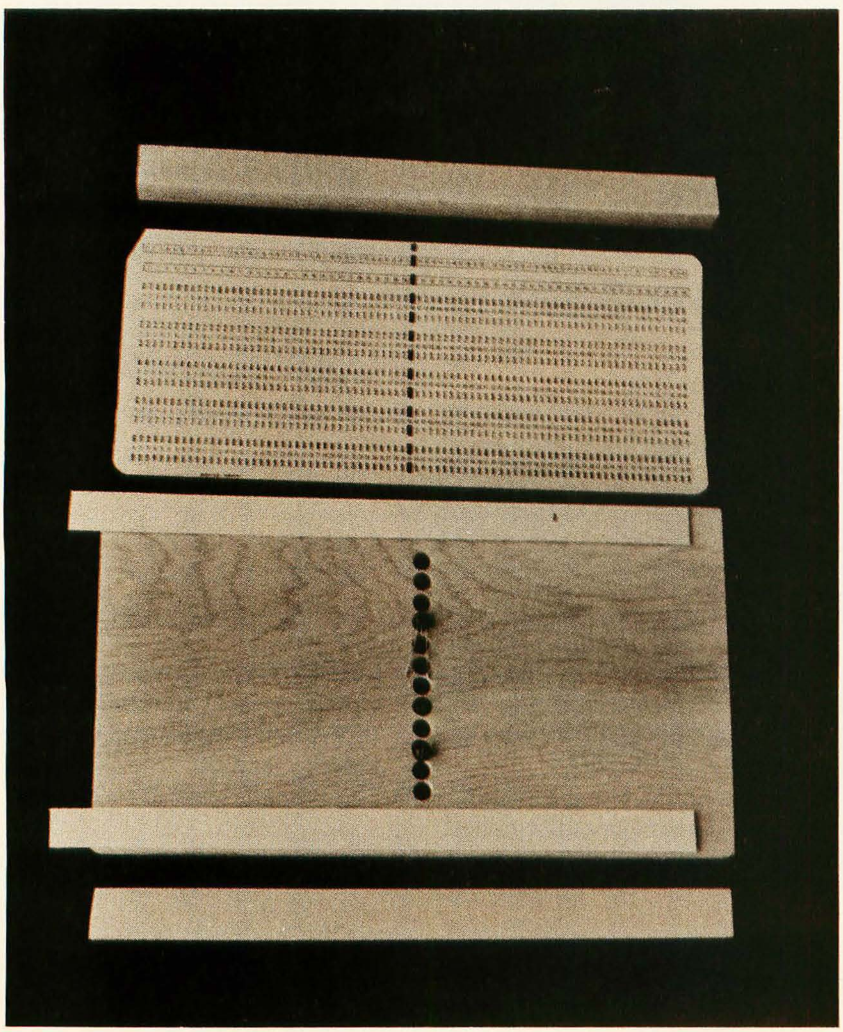
Circle 360 on inquiry card.

The Eclectic Card Reader

Anthony J Schaeffer
3510 Dunstan Dr
Bloomington IN 47401

Recently, upon completing an LD-14 version of the PDP-8 minicomputer, I encountered the common problem of data entry: all that I had were the panel switches and a softwareless cassette recorder. (See "A Tutorial Training Computer," January 1977 BYTE, page 76. This is a useful tool for learning digital electronics.) Paper tape provides the usual solution to this problem, but it was difficult to extract paper tape from the large system I use. The only solution seemed to be to follow the big fellows and use punched card input. Enough details of my design of the card reader follow so that an enterprising soul can modify it for other uses. I hope that a manufacturer will produce and market an inexpensive people powered card reader of similar design. Punched cards are too pervasive for small computer users to ignore forever.

Photo 1: The parts of the reader laid out before assembly.



Standard punched cards have 80 columns and 12 rows. Simple readers usually read one column of 12 bits at a time; the reading is typically done by shining a light on the card and sensing a 1 where there is a hole and the light can get through. Since there are 80 columns, some clocking method must be arranged to determine when a column is aligned with the detector and ready to be read. In a reader where the card is moved by hand at nonconstant speed, the only effective method of obtaining clocking is to dedicate one row on the card to being a clock row. When it is aligned, the other rows are aligned and data can be read. Naturally, every hole in the clocking row must be punched, and the clocking row is not available for data, so there are only 11 bits of data per column. Since most computer systems that use a reader of this simplicity are based on eight or 16 bits, the loss of one bit out of 12 is not a severe loss. One simply punches eight data bits per column and has four bits left for clocking and error recovery.

Figure 1 shows the mechanical detail of my design. The wood parts were cut from a scrap 1 by 6. (Actually 3/4 by 5 7/16 inches or 1.9 by 13.8 cm.) First I cut the board to the length of a card. Then I trimmed 1/2 inch (1.3 cm) off each edge to make the top guide rails. The finished base was about 4 1/4 inches (10.8 cm) wide. A card with all 12 holes punched in column 40 is the only precision piece, and it provides the alignment for the reader. (Nine holes suffice to read eight bits of data plus one clock bit.) Using this card as a template, mark the board and drill 3/16 inch (0.5 cm) holes to accommodate the phototransistors. This

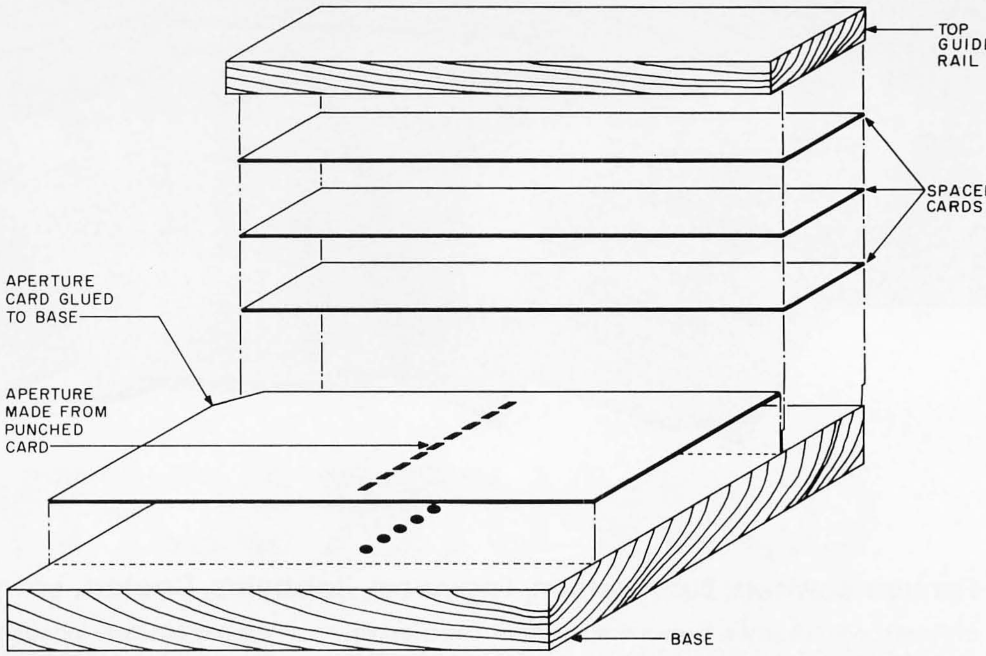


Figure 1: Construction of the author's homebrew punched card reader. The base is drilled for photo transistors (see detail of mounting in figure 2). Above each hole is an aperture made by a punched hole in the aperture card, which is glued to the base. The top guide rail is glued to a stack of spacer cards.

drilling should be done accurately; a sharp bit will produce clean holes. After the holes are drilled, glue the aperture card to the board. I found watered down white glue to be easy to use.

To form a slot in which the card can move freely, build spacers at the top and bottom edges of the reader. These can be constructed by gluing three cards together. When the glue is dry, cut them lengthwise with a sharp knife and a straight edge. Smooth them slightly and glue the spacers snug against the aperture card as shown in the figures. Before attaching the top guide rails, spray paint everything flat black to reduce stray light that could shine through the reader body into the phototransistor. Finally, glue the top guide rail and nail in place with about 1/8 inch (0.3 cm) overhanging the aperture card to form the guide. See the end view in figure 2.

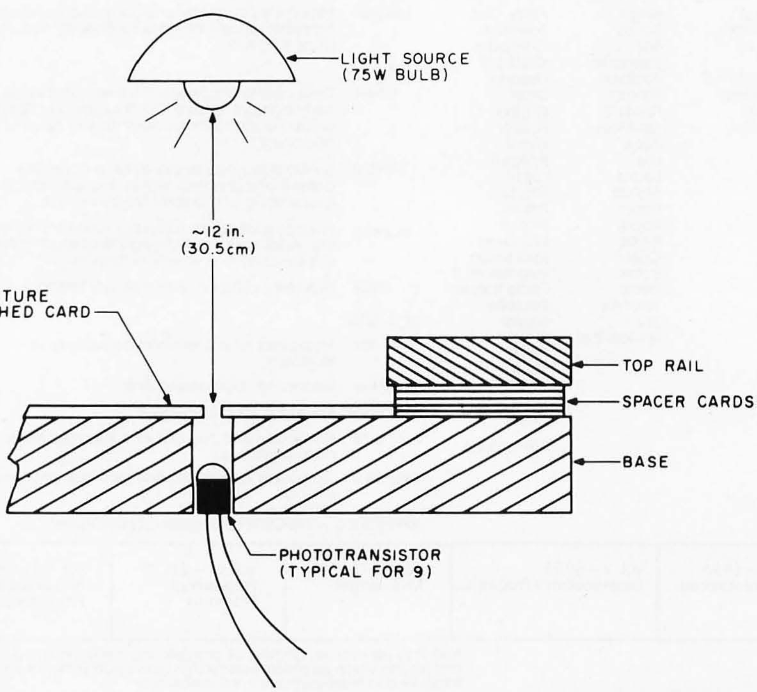


Figure 2: Cross section of the card reader. The holes in the aperture card are lined up with the drilled holes for the photo transistors. (In this drawing only one of nine photo transistors is shown.) The top guide rail forms a notch which keeps the card being read from wandering.

Figure 3 shows the basic circuit. I used Fairchild FTK0031 phototransistors which I purchased from James Electronics. I believe these are actually FPT-100 that are not being used in new designs, so Fairchild has put them in an inexpensive kit for experimental usage. These devices usually have no connection to the base, so I cut off the base leads. The pull up resistor holds the inverter input high when the transistor is not being illuminated. It also controls the sensitivity of the circuit. It should be small enough to hold the input high when the phototransistor is covered. About 2.2 k ohms for normal TTL seems to work well, but in the breadboard stage I found that no resistance also worked. Smaller values can be used to reduce the sensitivity. As the circuit stands, it will not switch reliably because noise will cause the inverter to switch off and on as the light on the phototransistor increases or decreases through the threshold value. This "bouncing" can be eliminated by using a Schmitt trigger inverter or gate: 7413, 7414 or 74132 (see "Look What You Can Do. . . with an Edge as a Cue" by Ralph Tenny, August 1977 BYTE, page

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- Enter ASCII characters in memory
- Fill memory with user defined byte
- Move block of code to different address in memory
- Verify discrepancies within two blocks in memory
- Locate a string in memory
- Branch to user defined routine
- Go to and execute user defined address with two breakpoints available for debugging
- Hexadecimal arithmetic
- Question input ports and command output ports
- Tape Cue; cassette on/off
- Read tape cassette file in memory (bias available)
- Write file onto tape-cassette
- Memory test for bad chip
- Calculate top address of RAM

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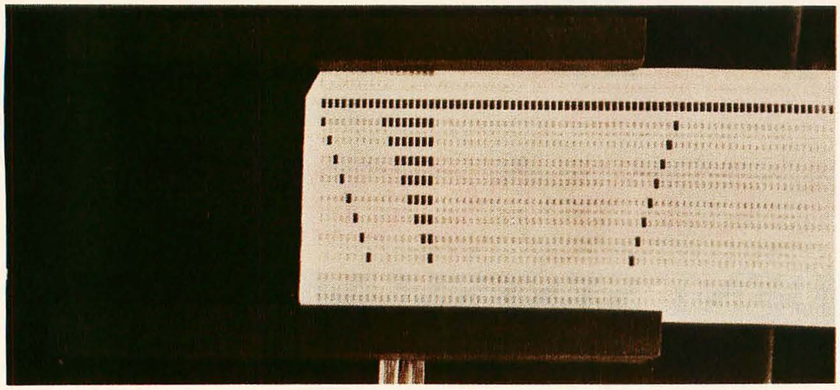


Photo 2: A view of the completed card reader, with a test card partially slid through the device. Note the timing track punched along the top row in every column, with arbitrary test data in several columns. Note also how the wooden guide overlaps the card at the top edge of the picture.

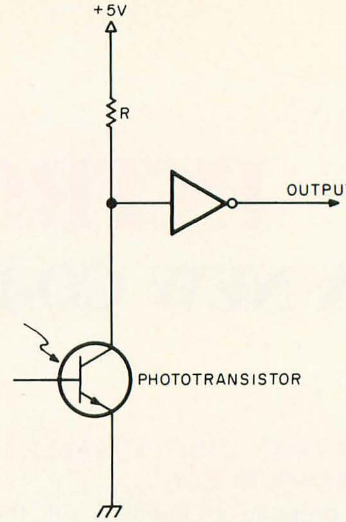


Figure 3: Detail of the photo transistor circuit used for the reader. The resistance R controls the sensitivity of the circuit. About 2.2 k ohms is the nominal value for the eight data zones of the card, and the single "clock" row (every column punched) is adjusted to a lower sensitivity by using a smaller resistance value. The lower sensitivity of the clock track is used to delay the clock pulse slightly to guarantee that the data is stable.

About the Author

Anthony J Schaeffer holds a PhD in applied mathematics from the University of California and is currently PLATO site director at Indiana University, Bloomington campus.

120). I used a Schmitt trigger only on the clocking bit, but it would be best to use one on all of the bits. Also, low power Schottky integrated circuits have higher input impedances and will give greater sensitivity.

It is essential that the clocking bit switch cleanly. Also, it must be the last one to come on and the first to go off. The data bits can bounce a little, as long as they have stabilized before the clock comes on. The data bits do not need to extinguish between adjacent punched columns, as long as they go off in an unpunched column before the clock comes on. I achieved this by adjusting the position of the light so that the data bits just extinguished between adjacent punched columns. Then I reduced the sensitivity of the clocking bit until it would just come on reliably for every column. This seemed to give reliable results.

For the record, I used a 75 W bulb in a goose neck lamp about 12 inches away from the reader. Phototransistors respond best to an ordinary filament light bulb or to an infrared LED, but visible LEDs and fluorescent lights do not work well.

Many variations on this reader are possible. An end-of-card indicator would be a useful addition. In my second version, I wanted to be able to read all 12 rows as data, so the clocking information could not be on the data card. To get the clock, I had the data card push a clock card past a second read station. The alignment was achieved by punching both the data station card and the clocking station card in column 40. These two cards were glued side by side on the board, so when the data card pushed the clock card, corresponding columns were aligned over both stations.■

Assembling the ADM-3A

Paul Franson
115 Fancher Ct
Los Gatos CA 95030

When I decided to acquire a personal computer system, I noticed that much desirable equipment is available in kit form at substantial savings over assembled cost. It's always tempting to save money, but like many others, I wondered if the savings were worth the trouble. Are the kits suitable for building by any computer enthusiast or does it take a dedicated and experienced hardware enthusiast to do the job? How hard is it to build a kit? Will the equipment work after it's assembled? And who fixes it if it doesn't work? A $200 savings doesn't mean much if you end up with a piece of gear that doesn't work and can only be fixed with great difficulty at substantial cost.

I had already acquired an assembled microcomputer, but decided that I needed something more than the limited hexadecimal keyboard and display. The obvious answer was a video terminal, and Lear Siegler's ADM-3A intrigued me. It is widely used in industry (I see them in my work), has every feature you could expect in a video terminal and is available at a substantial savings for the home constructor.

I decided to take the plunge with the kit. If you have considered buying and assembling this or any other kit, you might be interested in my experience. To save you from excessive suspense, I'll tell you now that it wasn't a bad job, and the terminal worked the first time I turned it on. Nevertheless, I did run into some problems and I suspect that others who build this and related kits will have similar experiences.

Some ADM-3A characteristics should be considered before discussing its construction. Lear Siegler markets it as the "dumb" terminal, which turns out to be a very smart move. This lowly label serves to set it off from the expensive and much balleyhooed "smart" terminals being used more and more in distributed computer systems. The smart terminal contains a certain amount of computer power, allowing it to greatly reduce the load on its host computer, which may be a long telephone call away.

The ADM-3A, on the other hand, is just what the hobbyist and many professional users need. It contains all the needed features, selection of a variety of configurations with numerous small internal switches and options available for some other features.

Among the main features are its 12 inch (30 cm) video display, which can display 960 characters in 12 lines of 80 characters per line, or optionally, 1920 characters in 24 lines. The standard 64 character ASCII set is displayed in upper case, and all usual controls and punctuation are included. The characters are formed from the standard 5 by 7 dot matrix. Lower case display is one of the options available at additional cost. Like the extra display, the lower case characters are added by simply plugging in some additional integrated circuits and flipping an internal switch.

A big plus of the ADM-3A is its versatility, assuring users that it will work with any systems they are likely to have. Full cursor control is provided under local or computer control, with either reverse block or underline to indicate its position. Data can be entered from top to bottom or at the bottom of the screen with scroll upward like a typewriter. End of line is indicated with a beep, and the terminal can be set to start a new line automatically at the end of the line you are entering.

Both Electronic Industries Association (EIA) standard RS-232C and 20 mA current loop (Teletype) computer interfaces are provided, with an auxiliary interface for RS-232C printer, magnetic recorder or other device. Communications rate is selectable from 75 to 19,200 bps, surely a wide enough range for virtually any use. Full and half

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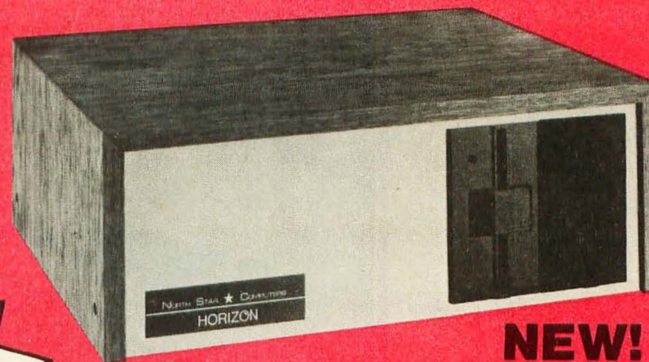
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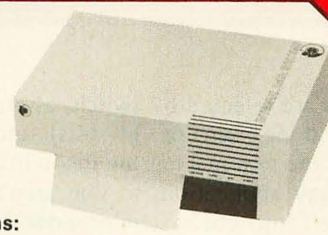
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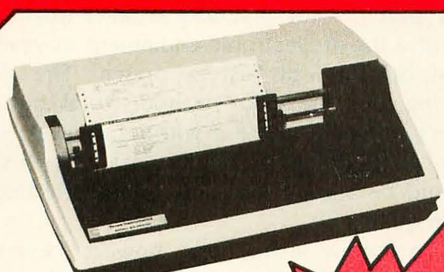
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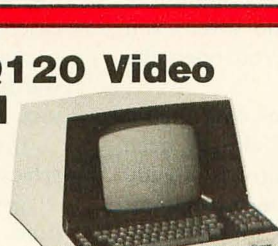
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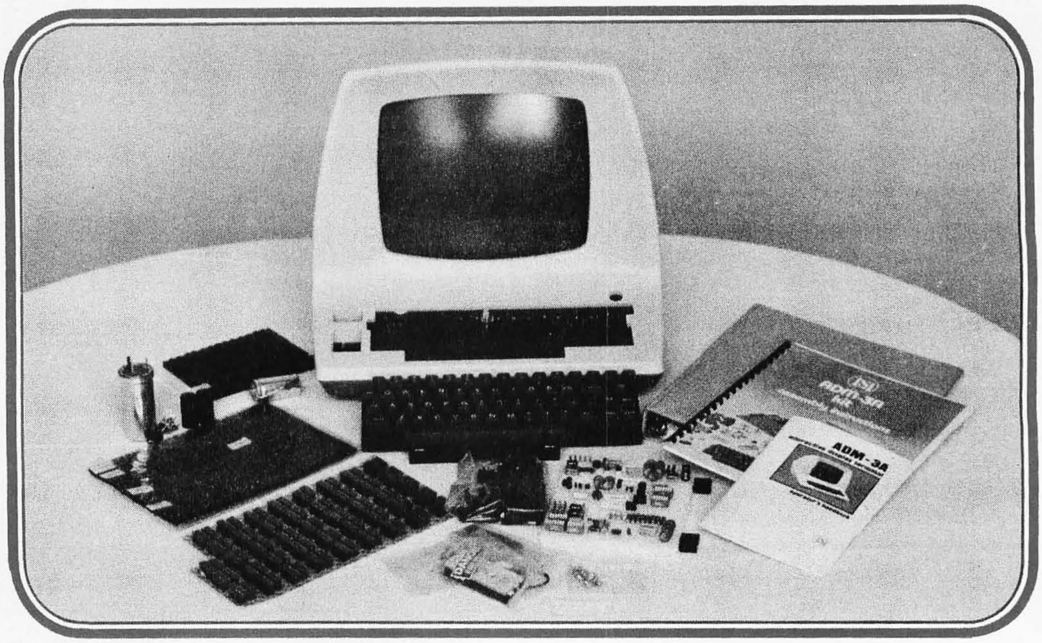


Photo 1: Lear Siegler ADM-3A "dumb" terminal kit. When the kit is unpacked, the various parts are grouped in convenient sections.

duplex modes are selected by switch, as are word length (nine, ten or 11 bits) and parity. Again, the terminal has the flexibility for virtually any application, so you aren't locking yourself into one system or mode of operation.

The individual builder of the kit doesn't go though all the tests, inspections and the burn-in cycle that Lear Siegler applies to its assembled equipment, but the design and components are the same quality as in their commercial units.

All Those Parts?

The first thing you notice when you get the terminal kit is its huge packing box. The terminal itself is not much larger than a typewriter with the video display on top, but the packing box could have a good size color television in it. The reason for the size is the careful packing for protection in shipping. You're not likely to find shreds and pieces of the terminal when you open the box.

The next surprise as you look over the kit is that much of the work has already been done for you. The video monitor is already assembled and mounted in the top half of the case, and the hefty power supply transformers, primary fuse, switches and cables are already attached. Even the end of line beep speaker is installed on the bottom (it drove me crazy trying to find it until I read the instruction book—more on that later).

The third observation as you look at the contents of the packing case is the shock when you see the vast number of integrated circuits in the kit. Sockets are provided, thank goodness, but it dawns on you that you are going to have to solder every lead of each of the almost 150 sockets, plus the other components mounted on the circuit board. That's a lot of soldering (unless, of course, you have a wave solder machine handy) and the spacing between sockets is pretty tight.

Time for second thoughts? No, it turns out that it's not that bad a job. I used to build a lot of electronic equipment in years past, but I'm a bit rusty at present. The soldering took me about six hours total, but I don't think I'd tackle it without some experience. Building a simple Heathkit first would be a good idea and would probably help quite a bit.

Do follow instructions, however. Every kit I've ever built has warned not to jump ahead in assembly, and I always do something that looks right to me and end up cursing when I find out that I goofed. In this case, it was soldering two small dual-in-line package switches (with 14 leads) in backwards. Correcting the problem was a nasty job.

Installing and soldering the sockets themselves was fairly straightforward. The manual suggests that you insert all of the sockets, hold them down with masking tape, then turn the board over and tack each socket down by soldering in two diagonal corners. Then you remove the tape, and if any socket isn't flat against the board, it can be seated easily by softening the solder and pushing the socket in place.

After all the sockets are in position comes the big job: soldering each terminal to the board. I suggest you take it in a few sessions

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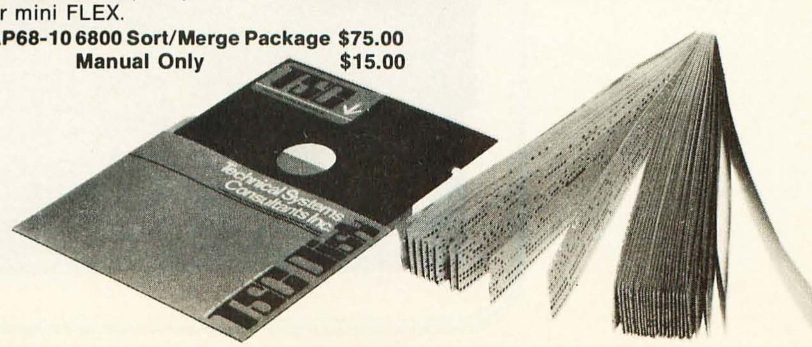
36 Additional Disk Utility Commands

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with breaks in between. Also use a good, hot, sharp pencil iron and very thin, quality solder. Eutectic is best, but 60/40 solder will do about as well. Very little solder is needed, and you have to be careful that the adjoining pads aren't shorted because of the close spacing. Note that the iron tip should touch the plated through pad on the board, not just the socket lead. This forces the solder to wick into the hole rather than balling up on the lead, which can hide a bad joint.

After all the sockets have been soldered in place, and then carefully checked the next day, it's time to start on the other components. Everything in the kit, except the premounted parts I mentioned before, is mounted on one large circuit board. Even the keyboard is mounted on the board, which is of high quality glass epoxy.

The miscellaneous components cause the only real problems in the kit. Some of them are not well identified, making placement a bit confusing at times. Component locations are silk-screened on the circuit board, and rough diagrams are included in the instructions, but I'll admit that I had to scratch my head more than once. A few of the board notations are wrong: 1 instead of 0.1 and 10 instead of 10 k. But they weren't too hard to figure out because the components are grouped in assembly and because there are relatively few discrete components used in the terminal. (I had one capacitor left over, by the way. That always irks me, but the terminal works so well I surmise that there is no need to worry.)

The next step is to mount the keyboard in place. The assembly manual warns you not to unpack it until you're ready to mount it in place, since the terminals are very delicate and easy to bend. Unfortunately, like everyone else who gets the kit, I had to take the keyboard out and poke at the keys, and sure enough, I bent the terminals. I did not enjoy straightening them over and over until they were lined up perfectly, but I finally got the keyboard in place. So *take their advice* and don't unpack the keyboard until needed.

After the keyboard, the sockets and all the other components are soldered in place, but before the integrated circuits are installed in their sockets, the power supply voltages must be checked — then you turn off the power and install the components. This is likely the only place you'll need to use an electronic test instrument. Believe it or not, this was a long and tedious job. Note that only the suffixes of the devices are shown and by the way, the 9LS04 or N74LS04 was labeled LS04 in my kit.

The tricky part, however, is seating the components without bending the leads, missing the holes or puncturing your thumb. The devices from different manufacturers are made with different materials, which also complicates things since the best technique for the stiff National integrated circuit leads doesn't work best for soft Signetics devices. A good method is to seat one row,

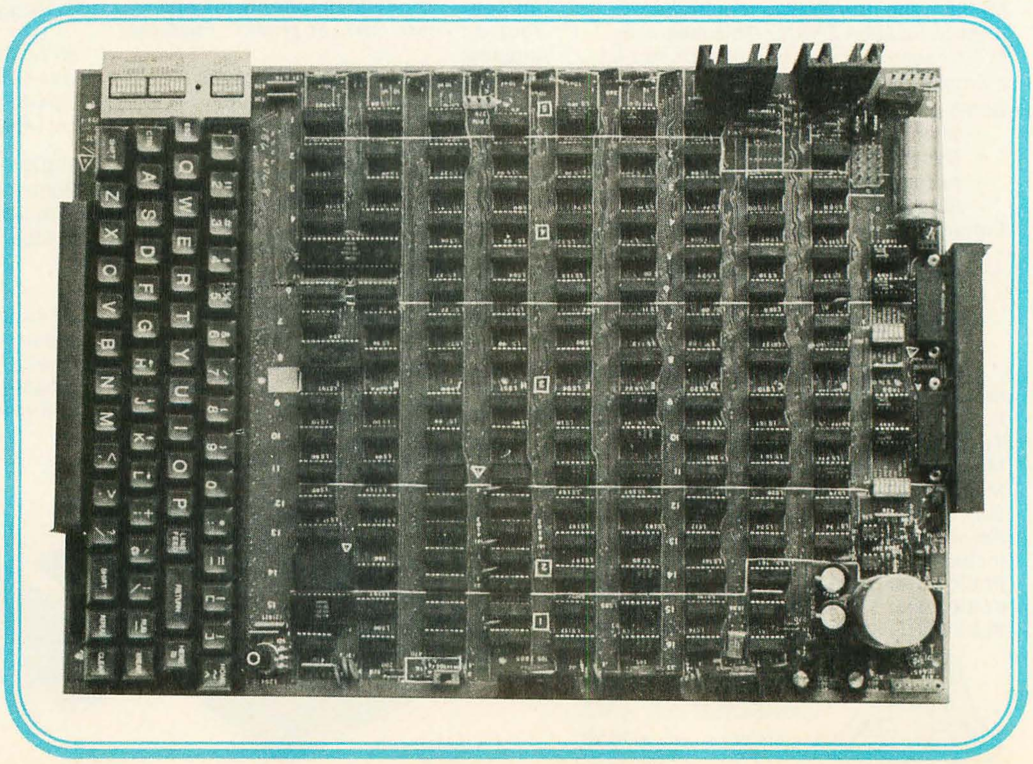


Photo 2: Most of the circuitry is assembled on the large printed circuit board shown. This includes the keyboard and power supply.

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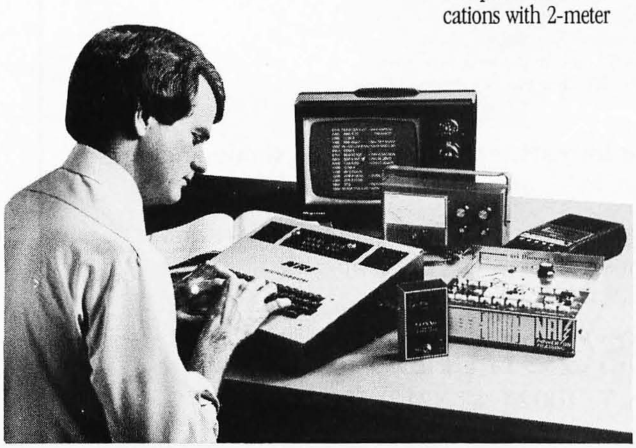
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then use a plastic credit card to force the other row in line. I broke one lead and very quickly soldered on a replacement, but I'm sure National Semiconductor would shudder at the thought.

Empty Sockets

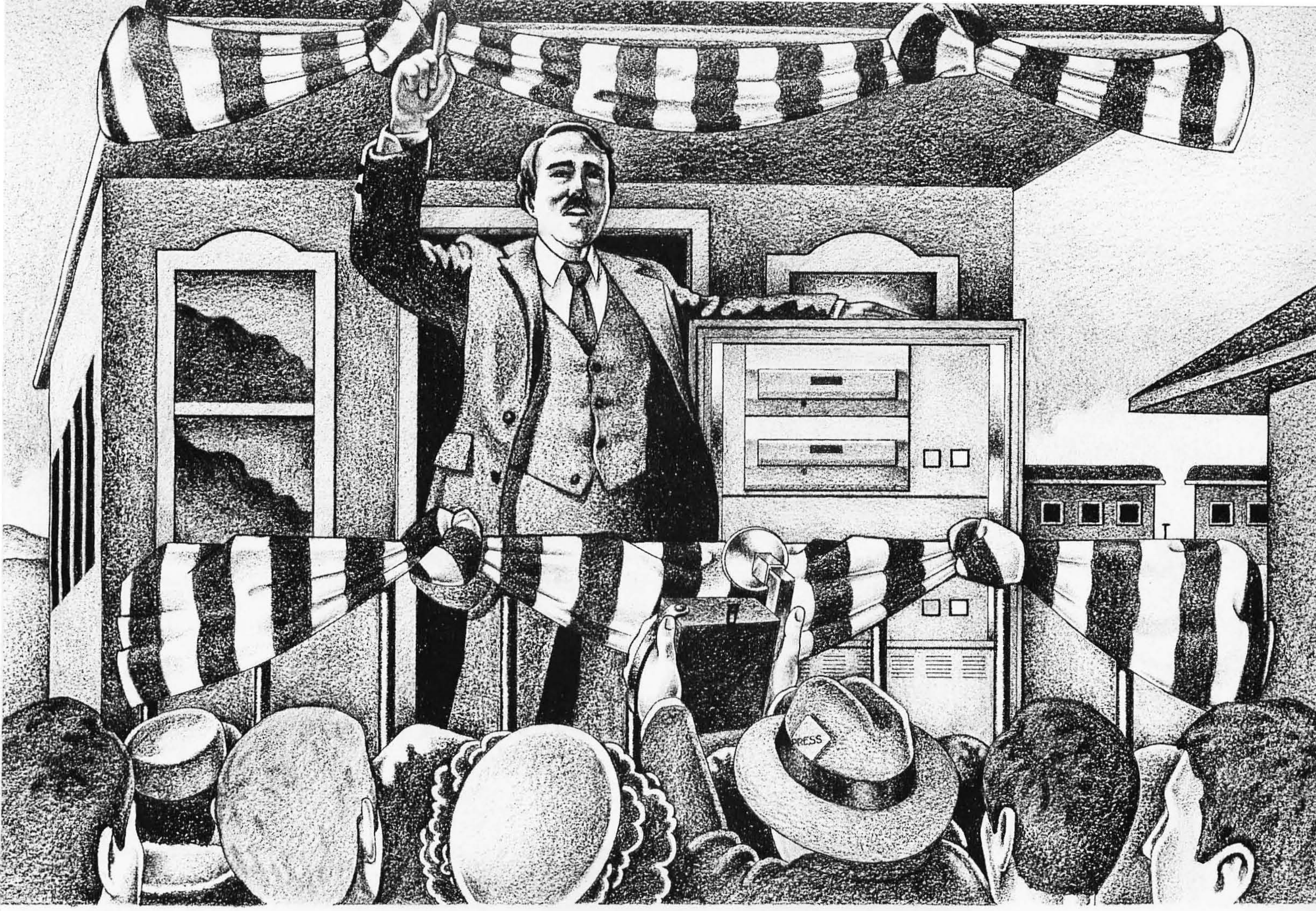
Depending on the options you buy, empty sockets may be left after you've installed all integrated circuits provided. Here again, the instructions are a bit cavalier, but you can figure out which ones should be vacant without much trouble. One position has holes drilled for a socket, but no connections to the pads, and sockets are provided for devices even if they aren't included. This simplifies installation of optional features at a later time.

One major option is 24 lines displayed on the screen instead of 12. This calls for six additional 1 K byte memory circuits and throwing a switch. Another option is lower case letters as well as capitals. This calls for a special character generator plus two more memory devices. This character generator, incidentally, is the only proprietary circuit in the terminal. All others are standard parts that are widely available.

The last important step in building the terminal is turning on the power with all components in their sockets and the monitor connected. I was amazed to find that the terminal worked the first time I threw the switch. The surprise was no reflection on Lear Siegler, but because of doubts about my craftsmanship. After setting the internal switches for use with your computer, final assembly consists of simply closing the case and installing two screws.

The terminal works perfectly with my computer (presently a PACER using the 16 bit National PACE microprocessor). I didn't have to do any troubleshooting, but the comprehensive manual ought to take care of that if the unit should ever need repair. Lear Siegler doesn't service kits, but computer dealers should have facilities for repair.

In retrospect, the only hitches I encountered in building the terminal (other than the minor problems in component identification and location) were caused by not following instructions. A word to the wise, then, is to *follow instructions.* My total working time was about 12 hours; Lear Siegler suggests 20 as typical, and that would likely be true for someone with less experience. I'm very pleased with the terminal, and I think the work of building it was worthwhile.■



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There is a need for a hobbyist robot arm—a computer controlled manipulator for the small system owner. The criterion for such an arm is that it be comparable in price to other computer peripherals and that it be sufficiently versatile to offer experimenters an expansive vehicle for their imaginations. One of us (Keith) has a working prototype which is described in this article.

How big and powerful can we expect such a hobbyist arm to be? There is a rough correlation between size and expense, so we can expect it to be small. How small depends on the strength of our motors (not necessarily electric), how fast we expect the arm to move, and how much weight we expect it to carry. The specific trade-offs between speed, strength, and reach will be determined by the tasks we want our arm to perform. For industrial robots there seem to be basic choices of 5 or 6 foot arms using hydraulics, 4 foot arms using large servomotors, or 1 to 2 foot arms using small high performance electric motors. The hobbyist arm will probably be of the last type. Of course this relationship is by no means unyielding; novel designs or alternative motors (such as chemical muscles) might change these trade-offs substantially.

Have we defined an arm so small that it would be uninteresting? By no means — there are potentially interesting applications for all sizes of arms. In fields such as microsurgery or in the assembly of minute electronic parts, a breakthrough in small robots could prove invaluable.

The hobbyist arm is not likely to be at the forefront of a new technology, yet

A Hobbyist Robot Arm

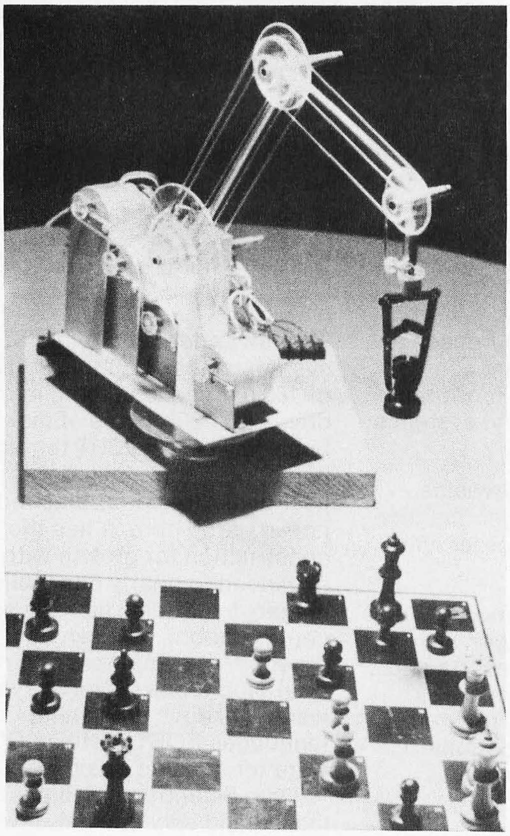


Photo 1: The robot arm moving a chess piece on a board. This photo shows how the arm can grasp one piece on the board without disturbing any of the surrounding pieces. (Photo by John W Baxter.)

it can provide a mechanism through which the experimenter might investigate the principles of robotics. This article describes a particular approach to the design and construction of one such arm. It is hoped that the result will serve as a starting point for subsequent robot arm designs and as a reference point in the discussion of mechanical manipulators for the experimenter.

The design constraints are to:

- Consist of readily available parts.
- Require a minimum of special tools or skills to assemble.
- Be inexpensive to assemble.
- Possess the strength to lift playing pieces (eg: chessmen, Monopoly pawns or checkers).
- Provide a readout of the position of each joint.
- Be easy to repair.

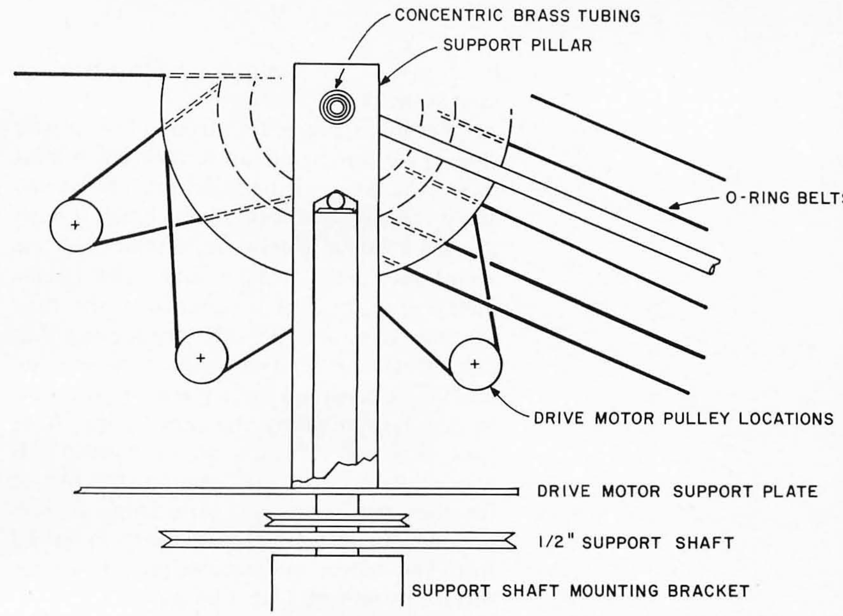
The basic mechanical framework of the arm is a major stumbling block. Tim's approach to the problem was to buy a jointed lamp (Luxolamp). It provides six readily available axes that need only be motorized. There is no interaction between the joints (moving one joint will not cause another to move). It is reasonably inexpensive (about $20) and universally available.

The hobbyist arm must also perform adequately to be useful in a specific application.

Moving chess pieces on a chessboard was chosen, since it offers a simple task in a rectangular coordinate system requiring the arm to move pieces in an obstructed space.

This task helped define the necessary axes of the machine. An axis is a joint: either rotational, as in an elbow or wrist, or prismatic, as in a telescope tube.

Three axes are sufficient to allow an arm to touch any unobstructed point within the limits of its reach. If points are permitted to be obstructed from certain directions or if the wrist must maintain a fixed angle with respect to the real world, more axes are needed. In the case of a chess playing robot it is desirable to lift pieces vertically without knocking down surrounding pieces. For this reason, three axes are not sufficient.



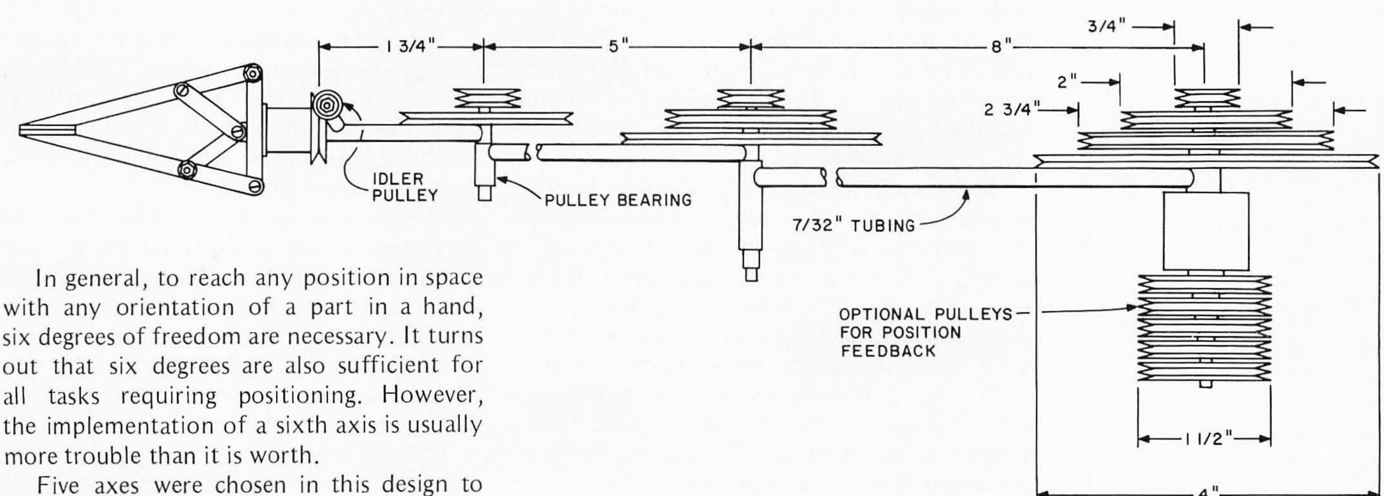


Figure 1: A design sketch of the hobby arm. The main structure of the arm is brass tubing. The pulleys are constructed from Plexiglas. The hand is made of sheet aluminum and activated by a solenoid mounted on the arm. All of the driving motors for the arm are mounted on the base plate of the assembly.

In general, to reach any position in space with any orientation of a part in a hand, six degrees of freedom are necessary. It turns out that six degrees are also sufficient for all tasks requiring positioning. However, the implementation of a sixth axis is usually more trouble than it is worth.

Five axes were chosen in this design to provide additional flexibility in roughly the same configuration as the human arm: rotation about the waist, shoulder, elbow, wrist, and rotation along the wrist. This configuration allows an easy visualization of the arm's capabilities because it is similar to one's own arm.

One final word about the factors that shaped the design: the motors one uses define the working limits of the arm to a great extent. If the motors can deliver 10 ounce-inches of torque at one revolution per minute (very respectable for most common small geared motors), the working weight at the end of a foot long arm would be less than 1 ounce — providing the weight of the arm itself is kept to a bare minimum. Clearly, one would prefer under circumstances like this to avoid mounting the motors on the arm so that they have to lift themselves. For this reason we mounted the motors behind the arm. Their torque is transmitted to the joints by means of concentric pulleys and rubber belts.

The framework of the arm is constructed of thin-walled brass tubing purchased from a local hobby store. This tubing comes in square or round cross-section and should prove highly useful to the beginner embarking on an original design. Consecutive sizes differ in radius by their wall thickness and hence slide smoothly into each other with very little play. This characteristic is made use of in the shafts for the concentric pulleys transmitting the torque of the motors along the arm. Lengths of the tubing are also used for the struts of the arms. The brass, in tubular form, is very rigid: though heavier than other materials, it makes up for its weight in the ease with which it may be fastened to other bits of tubing by soldering. To make a joint, the end of the tube is filed to fit smoothly, without gaps, against the radius of the pulley shaft bearing. For the joint to be strong, the solder must not have to bridge gaps between the brass surfaces, but should

be drawn in by capillary action when the joint is heated.

The pulleys are cut from clear plastic (Plexiglas) purchased as scrap from a glass shop. The edges of the pulleys can be turned and given a groove with a small lathe, though the same job might be done somewhat less accurately with a hand file. The largest pulley at each joint is fastened to the strut of that joint and provides torque for that axis of the arm. The smaller pulleys are double-grooved and serve merely to transmit torque farther along the arm to the other axes. The size of each pulley corresponds approximately to the amount of torque for that particular axis. The larger pulleys provide an effective reduction in speed from the motor pulleys and provide a large surface to prevent belt slippage.

The rubber belts are clear neoprene with nylon cores. The belting material may be purchased under the name of O-ring cord. The cord is cut to length and the ends joined by melting them in a flame and pushing them together. This method yields a remarkably strong joint.

The support pillar for the shoulder joint is machined out of a block of aluminum. An alternative is to make it out of laminated scraps of Plexiglas. In this case the motor support plate may also be made of Plexiglas and glued, instead of screwed, to the support pillar. The concentric brass tubing which forms the pulley shafts for the shoulder axis is extended to provide a place for pulleys to be used for position feedback potentiometers if a closed loop servosystem is desired.

The waist axis is mounted on a single steel ball resting on top of the support shaft about which it pivots. A pulley fastened to the support shaft is driven by a motor facing down through the motor support plate to provide rotation about the waist.

The motors used in this version of the arm are AC synchronous bidirectional timing motors. They are inexpensive ($4), though their power is near the minimum necessary for adequate performance. Power is applied to the windings with a 90° phase difference. This is accomplished by the use of a series capacitor. Shorting this capacitor causes the motor to lock, providing a brake to hold an individual axis still while others are moving.

The fingers are cut from thin aluminum sheet and make use of a small solenoid with an alnico magnet plunger to actuate them. The wires are looped down the arm struts externally.

The entire arm is mounted on a 1 inch pine block with the wires from the motors terminating on a barrier strip along the back edge where an interface to a computer or a simple switch box may be connected. The plate that the motors rest on is mounted off-center so the arm has a greater overhang and therefore the largest possible unobstructed reach. The support shaft mounting bracket is mounted against the front edge of the pine block.

The small pulleys for the drive motors are epoxied directly to the motor shafts. If a method could be devised to allow these pulleys to be removable, it would facilitate experimentation with the drive ratios. In the present design, the arm may be disassembled down to the individual pulleys and struts unless the feedback pulleys have been installed, in which case the shoulder pulleys and the support pillar become an integral part.

The arm is capable of lifting a 1/2 ounce and positioning it to within a 1/2 inch radius. Drilling out the extra material from the concentric pulleys and counterweighting the upper arm should improve the lifting power somewhat.

The interaction of the joints (how the movement of one joint affects the position of the other joints) may be calculated and removed if the arm is to be computer-controlled. The interaction is such that joints further out from the joint being moved maintain the same angular orientation in space. Thus, if the hand is initially vertical to the plane of the table and the shoulder joint is moved, at the conclusion of the motion the hand is still vertical. There is no interaction from the waist axis or the wrist swivel axis, though wrist swivel is acted upon by the previous axes. For this constant angle effect to apply, the initial and final pulley for a joint must be of the same size. In practice it is desirable to maintain a uniform radius for the pulleys of a specific axis in order not to unnecessarily limit the torque transmitted because of slippage on a smaller pulley.

As with many types of design, this first working model suggested a number of areas of possible improvement. The first area is the motors. More powerful motors would be better, and at this point likely candidates are small stepping motors. Their price is high but they offer impressive torques along with the possibility of open loop control and straightforward interface hardware.

The elasticity of the belts, though small, offers another area where some additional thought might prove rewarding. A number of manufacturers sell small toothed belts

that would permit higher torques, with an increase in the complexity of the pulleys. Perhaps the simpler solution of doubling up the pulleys might be the answer.

A more powerful grip in the fingers without making them too heavy (as a bigger solenoid implies) would be another useful improvement. Perhaps an additional set of belts would work in this case also, with a gripper motor on the motor support plate.

Using the Arm

Eventually the arm will be connected to a microprocessor. There are two methods of controlling the arm. The first is open loop; the second is closed loop.

Open loop control requires a command from the computer that tells each axis where to go. It is assumed that the axes in fact reach these locations. The number of turns each driving motor takes to position its axis is determined through a minor feedback loop around the motors, or, in the case of stepping motors, by counting the number of step commands issued. This is the least expensive method but it requires high accuracy in the arm.

With closed loop control the position of the arm is monitored by the use of feedback potentiometers returning a voltage proportional to the position of the arm. This voltage is subtracted from a position voltage produced by the computer and the difference is used to drive the motors. When the signals match, the difference is zero and the motors stop. In general, feedback tends to cover a multitude of mechanical sins. Accuracy in positioning with this method depends on the linearity of the feedback potentiometers. For this reason industrial arms often use optical encoders instead of potentiometers for feedback signals. An optical encoder produces a digital output by means of a series of light beams and photodetectors interrupted by a rotating disk which selectively transmits or blocks the light depending on its position. Such encoders cost several hundred dollars. A challenge to readers would be to come up with a scaled-down version of these to use with a hobbyist arm.

Computer control allows velocity and acceleration information to be used to obtain better control of the dynamics of the arm. Nonlinear feedback potentiometers can be compensated for by using correction lookup tables. Interaction of joints can also be removed. Finally, the computer can be used to write programs for a higher level manipulator language where machine commands such as *move axis* are replaced with commands such as *move hand from A to B in a straight line*. Herein lies the future of robot manipulators.■

REFERENCE

Pieper, Donald L, "The Kinematics of Manipulators Under Computer Control," October 24 1968, CS116 AI 72, Computer Science Dept, Stanford University.

Sources of parts for the builder of small manipulators

O-rings (nylon-core, clear neoprene):
Winfred M Berg Inc
POB B
499 Ocean Av
East Rockaway NY 11518
(516) 599-5010

Miniature timing belts and pulleys:
Stock Drive Products
55 S Denton Av
New Hyde Park NY 11040
(516) 328-3300

Small motors:
North American Philips Controls Corp
POB 768
Cheshire CT 06410
(203) 272-0301

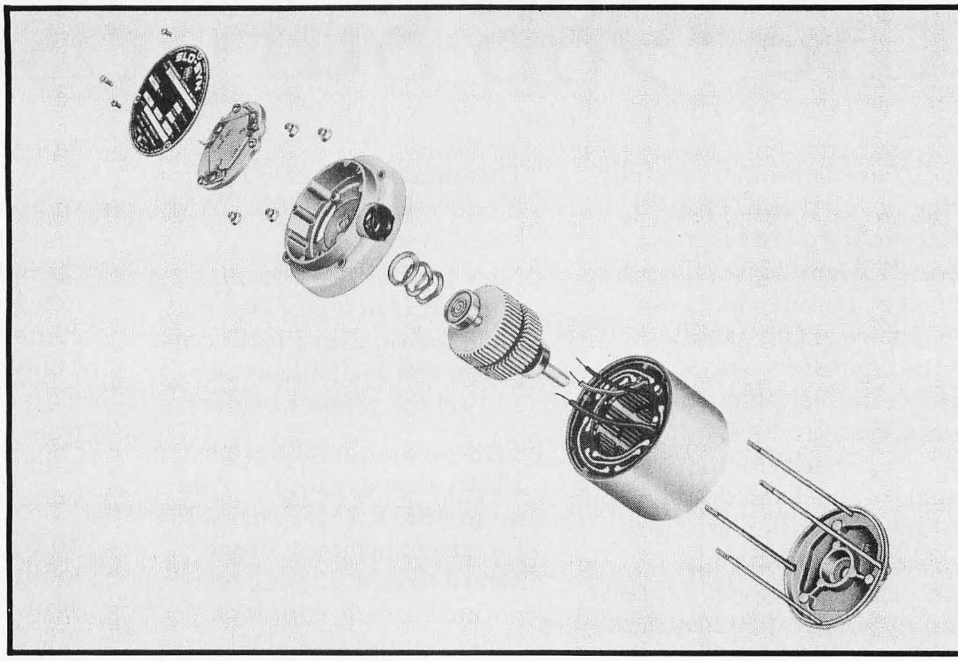


Photo 1: Exploded view of a permanent magnet stepper motor. The rotor has gear-like teeth on the ends of the magnet, making one hub north and the other south. The stator also has a set of teeth machined on its surface (photo courtesy of Superior Electric).

A Stepping Motor Primer

Part 1: Theory of Operation

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Introduction

Many times the computer experimenter would like to control the movement of some object by the computer, but servomotor systems are either too complicated or expensive. An alternative approach is to use a stepping motor, which in many cases is simpler in design and cheaper.

The only major problem with stepping motors is understanding how they work and how to drive them efficiently. This article describes what stepping motors are and how to use them. Since most applications involve the use of either the permanent magnet or variable reluctance type of stepping motor, the article concentrates on these two types. They can vary from a light duty stepper the size of a quarter to an eight inch diameter (.64 to .32 cm), one horsepower motor.

What Is a Stepper Motor?

A stepping motor is a motor possessing the ability to rotate in either direction as well as stop and start at various mechanical rotational positions, and whose shaft (rotor) moves in precise angular increments for each input excitation change or step. The displacement is repeated for each input step command. The result of this type of movement is the motor's ability to accurately position the rotor in a known repeatable direction.

The stepper motor allows control of position, velocity, distance and direction. Because each step moves the shaft to a known position, the only shaft position error (regardless of distance or direction of movement) will amount to the single step accuracy. This accuracy is generally 5 percent of one step. The number of steps in each revolution of the shaft varies, depending on the intended application.

Stepper motors are typically available in steps-per-revolution sizes of 200, 180, 144, 72, 24 and 12 steps per revolution. This gives an incremental shaft angle per step of 1.8°, 2.0°, 2.5°, 5.0°, 15° and 30°, respectively. Each motor is built for one particular step angle. They may be run at one-half the step angle, but at a reduced torque.

Most stepper motors are constructed with windings for 2, 3 or 4 phase operation. The bifilar winding, however, differs in that it has twice as many windings as the standard type. The advantage of this type of motor is that it gives better high speed performance

GLOSSARY OF STEPPING MOTOR TERMS

Back EMF: voltage generated by the motor that opposes the polarity of the voltage applied to the motor. EMF (electromotive force) increases as the speed of the motor increases until it causes the motor to lose synchronism.

Bifilar: special type of permanent magnet motor with two windings on each stator pole. The advantages: requires only one power supply, allows a simpler drive and has higher performance characteristics than a standard motor. This motor is manufactured by the Superior Electric Company.

Closed Loop: operating mode in which the drive or computer receives a signal from the sensor which tells what position the motor or actuator is in and which is used to improve control of the system. In all but very high performance systems, this form of operation is not needed.

Damping: reduction or elimination of oscillations or overshoot of the rotor in a move. Different types of damping methods used include mechanical, electrical and viscous.

Detent Torque: torque present at standstill of a permanent magnet stepper motor when the motor is turned off. There is no detent torque in a variable reluctance motor. Same as residual torque.

Drives: circuitry which controls the stepping motor. This can include the power supply, control circuits, and output switching transistors.

Half Step: switching sequence in which the motor is moved half its normal distance per step. As an example, a 1.8°, 200 step per revolution motor would become a 0.9°, 400 step per revolution motor. When running the motor with this type of sequence, the average amount of torque is reduced to roughly 70 percent of full step operation. This mode, however, gives a finer resolution, less resonance effects, and higher speed capability.

Holding or Static Torque: torque required to move the motor shaft from standstill (zero RPM) position when at rated power.

Inertia: tendency of an object to resist changes in movement by an external force. It is expressed in terms of mass X length^2 (ie: ounce-inch^2 or kg-m^2).

L/R Time Constant: value used to determine how fast current can build up or decay in a stepping motor, obtained by dividing the inductance in the circuit path by the total resistance in that path.

Moment of Inertia: the inertia of an object when rotating about a point. It is given in units of mass X length^2.

Open Loop: operating mode of a stepping motor in which the position of the shaft can be determined exactly using only the information sent to the motor. Stepping motors have this capability, which makes them more attractive than DC servomotors in certain applications.

Pull-In Torque: the maximum switching rate at which a stepping motor can start running from standstill.

Ramping: gradual acceleration and deceleration of a stepping motor. Since stepping motors are limited to a given starting speed, the motor must be accelerated to maximum if it is to operate above the pull in torque.

Residual Torque: the force which holds the stepping motor shaft at a fixed position after power is turned off, due to the magnetic attraction of the rotor teeth to the stator teeth. It feels like a "ratcheting" movement when the shaft is rotated by hand.

Resonance: the speed range in which a stepper motor's performance deteriorates. This is due to the physical construction and electrical characteristics of the motor. Various techniques can be used to reduce the effect of resonance on the system.

Rotor: the portion of a motor that rotates.

Speed-Torque Curve: graphic representation of the performance characteristics of a particular stepping motor and drivers. It usually shows the maximum speed/load ratio at which the motor is capable of operating. This graph is extremely useful when designing a stepping motor into a system.

Start/Stop Without Error: curve found on some speed versus torque graphs showing the maximum rate at which the motor can start or stop without losing steps or falling out of synchronism. This curve is usually given for a negligible load inertia.

Stator: the stationary part of a motor.

Step Accuracy: the position accuracy of a stepper motor, commonly given as a percentage of one step, since there is no accumulated error in a step motor. When a frictional load is put on the motor, the accuracy decreases.

Step Angle or Step: the amount of rotation of a stepping motor in response to one input command, expressed in degrees. Motors are made with a fixed step angle. 0.72°, 1.8°, 2°, 2.5°, 5°, 15° and 30° are typical sizes.

Stepping (or Stepper) Motor: a motor possessing the ability to rotate in either direction, and whose shaft moves in precise angular increments for each input excitation change or *step*.

Steps Per Revolution: the number of input steps required to rotate the shaft of a motor one complete revolution. To obtain the step angle of the motor from the steps per revolution, divide 360° by the number of steps per revolution.

Torque: force acting on an object at a certain perpendicular distance away from it, and tending to rotate the object. Torque has dimensions of force X distance. As an example, a two ounce force pushing an object from a 2 inch (5 cm) rod perpendicular to the force is said to have 4 ounce inches (0.0003 kg-m) of torque.

Torque to Inertia Ratio: ratio obtained by dividing the rated holding torque by the inertia of the rotor. The better the ratio, the better the performance of the motor.

Variable Reluctance Motor: a stepping motor that does not have a permanent magnet in the rotor. It therefore relies on the windings to create the forces to move the rotor. The variable reluctance motor, understandably, does not have any residual torque when it is turned off.

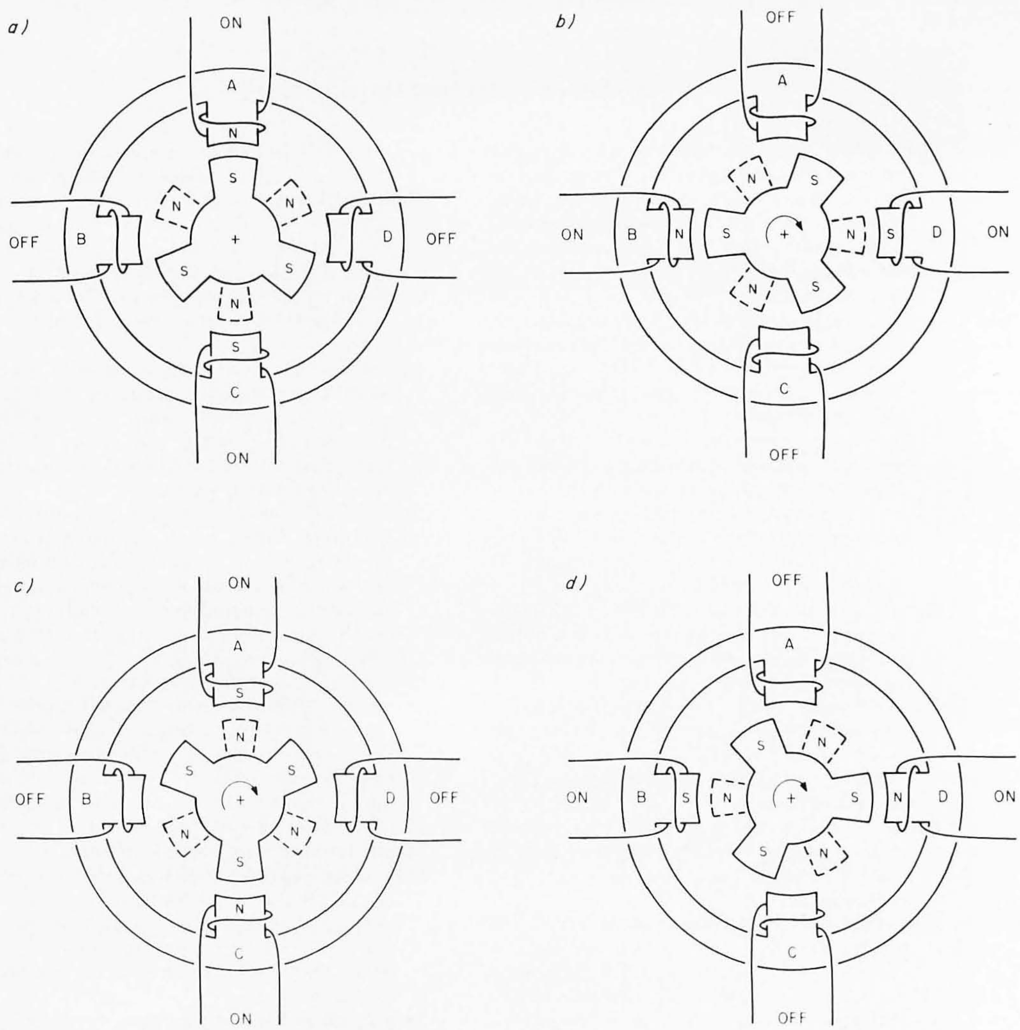


Figure 1: Energization sequence. Alternating power to the windings of the stator while changing the direction of polarity with each step produces movement in the motor. Reversing the sequence shown produces movement in the opposite direction. See text for a detailed description.

and simplifies the drive needed for the motor.

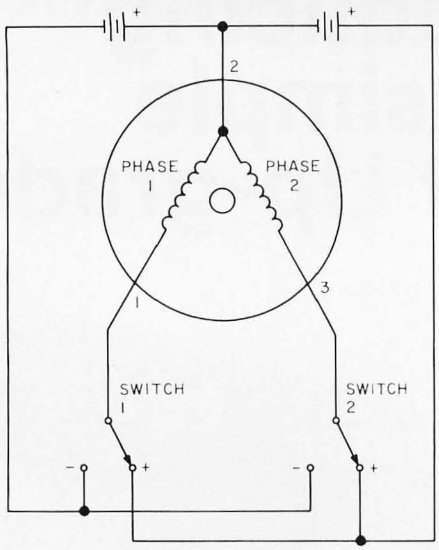
Stepper motors are generally controlled by a DC power supply and drive and logic circuitry. The drive provides the intelligence as well as the main key to performance of the motor. The degree of complexity of a drive can vary from a simple pulse translator to a high-performance unit with automatic acceleration and electronic damping.

Because the drive knows the shaft's position for all but high speed performance drives, the system can run in an open loop mode (ie: without the need for feedback position potentiometers, encoders or other transducers). This feature makes the stepper motor attractive over a DC servomotor system, which must be run in a closed loop mode. Stepper motors normally available are limited to less then one horsepower. However, the DC servomotor is available in larger power ratings, so it might be the choice for heavy duty applications.

Permanent Magnet Stepping Motor

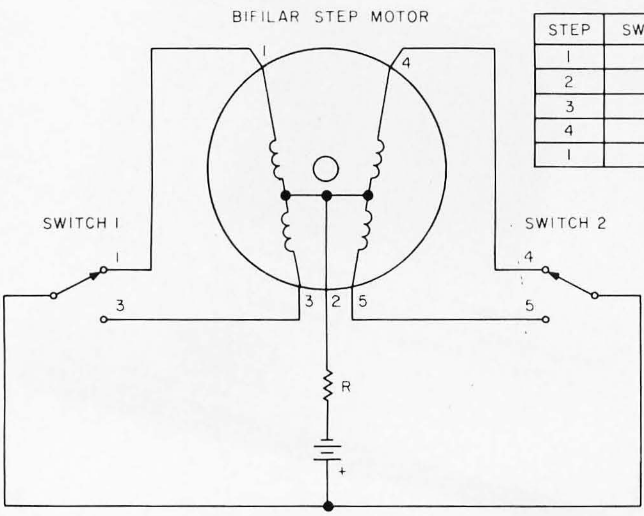
The permanent magnet stepping motor's basis of operation is taken from a basic permanent magnet characteristic: like poles repel while unlike poles attract. The rotor of a permanent magnet stepper consists of an axially-oriented magnet with two gear-like hubs on each end of the magnet, as shown in photo 1. The north end of the rotor has *teeth* that are 180° out of phase from the south end. The stator, or stationary part of the motor, also has teeth, as shown in photo 1; but the magnetic poles are generated by the windings. The number of teeth on the rotor is different from that of the stator, so that all the teeth on the rotor will never be lined up exactly with those on the stator. It is this fact that actually creates predicted movement in the rotor, since there is a magnetic attraction between the closest stator and rotor tooth. Even when the motor is depowered, the permanent magnet motor will hold its position, although at a low torque (called residual torque).

The energization sequence of the windings is fairly simple. Consider the south end of a rotor, as shown in figure 1: if pole A is energized as a north and pole C is ener-



	CLOCKWISE		COUNTERCLOCKWISE	
STEP	SWITCH 1	SWITCH 2	SWITCH 1	SWITCH 2
1	OFF	–	OFF	–
2	+	OFF	–	OFF
3	OFF	+	OFF	+
4	–	OFF	+	OFF

Figure 2: Connection diagram of a standard permanent magnet step motor and its switching sequence.



STEP	SWITCH 1	SWITCH 2
1	1	5
2	1	4
3	3	4
4	3	5
1	1	5

Figure 3: Connection diagram for a bifilar permanent magnet step motor and switching sequence. To run in the opposite direction, the stepping sequence is done in reverse order. Note that this motor requires only one power supply.

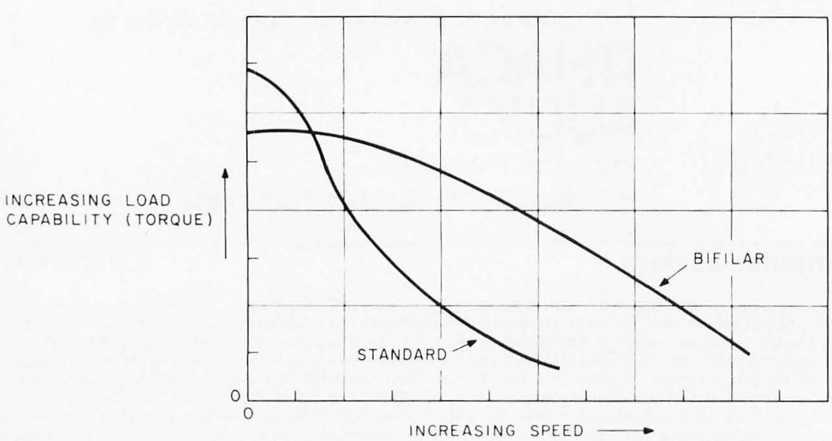


Figure 4: Performance of bifilar motor versus standard 3 lead permanent magnet motor. The standard motor has more capability at low speeds but quickly loses it as speed increases. Note also that the bifilar motor can run at a higher speed under the same conditions of load and drive.

gized as a south, with poles B and D not activated, the rotor will line up with pole A, as shown in figure 1a. If pole B is then energized as north and pole D as south, with A and C de-energized, the rotor will go in a clockwise direction, lining up with pole B, as in figure 1b. To take another step, the current is reversed from the original direction in poles A and C, and power is removed from poles B and D. This will make the rotor line up with pole C, as shown in figure 1c. To continue in a clockwise direction, power is applied to poles B and D with the opposite voltage polarity of before, as shown in figure 1d. The next step sequence is to apply power to poles A and C as in the original position. Repeating this sequence continues motion in the clockwise direction.

If the rotor is to be *stepped* in a counterclockwise direction, power should be applied in the reverse order. For more resolution in a practical motor, four more stator windings can be added, and teeth are machined on each stator pole and the rotor. In effect, each tooth acts as a pole. This is how the number of steps per revolution can be increased to 200 or more with a minimum number of windings. The windings on the stator are normally connected internally, with three to eight leads brought out for external connection. A simplified diagram of a standard 3 lead motor is shown in figure 2, along with the stepping sequence for clockwise and counterclockwise rotation.

Bifilar Stepping Motor

The bifilar stepping motor is a special variation on the permanent magnet stepper. In this case, there are twice as many windings as on the standard motor (see figure 3), but there are two windings on each pole. The wire is of a thinner gauge than the standard permanent magnet motor so it will fit in the frame size. The thinner wire results in a higher resistance, giving the motor a lower time constant and therefore increased high speed performance. Another advantage of the bifilar motor over the standard type is that the motor may be operated from a single-ended supply with a simpler drive. A graph of a bifilar motor performance versus a 3 lead motor is shown in figure 4.

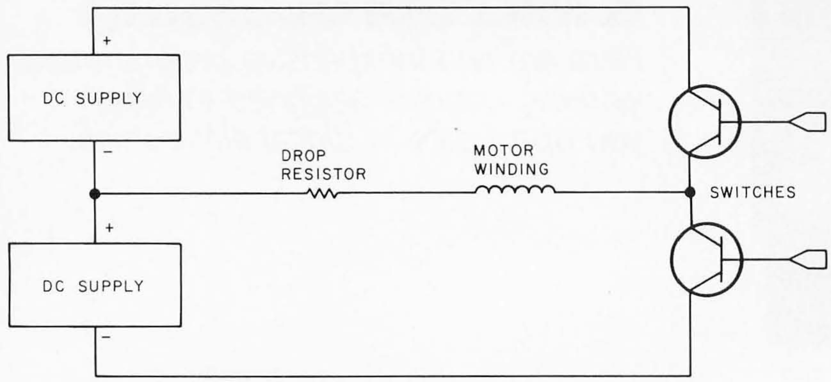


Figure 5: Simplified bipolar stepping motor diagram. This type of drive requires two supplies to run the motor.

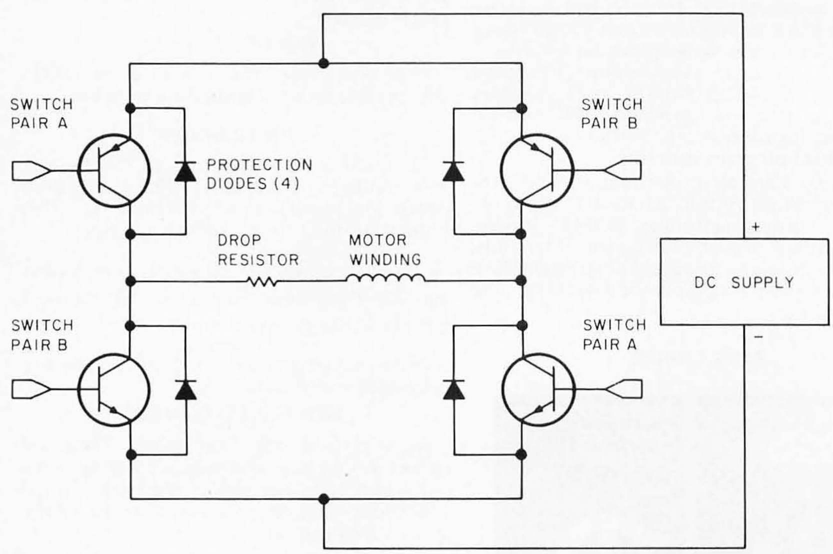


Figure 6: H drive configuration for one phase. By alternately turning on the switch pairs, the direction of current in the winding (hence the magnetization polarity) is reversed. This method requires eight transistors for a two phase drive.

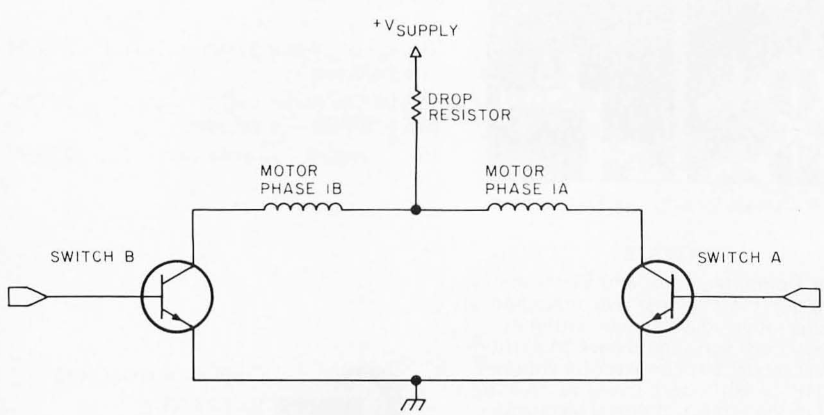


Figure 7: Simplified drive configuration for one half of a bifilar motor. The switches alternately turn on, causing the current to flow in one phase at a time. Each time the transistors switch, the magnetic polarity of the pole that the winding is on reverses. The drive requires another set of switches for the other phase of the motor.

Variable Reluctance Stepper Motor

The main difference between a variable reluctance motor and a permanent magnet motor is that the variable reluctance motor contains no magnet in the rotor. Since the rotor is unmagnetized, the rotor position is independent of the polarity of the stator phase excitation. This means that a single-ended power source can be used and bifilar windings are not required. Since there is no magnet in the motor, there is no residual or unenergized torque to hold the rotor at one position when turned off.

A comparison of permanent magnet and variable reluctance stepper motors shows that a permanent magnet motor has residual torque when windings are unenergized, a lower inductance that yields faster current response, and higher total inertia which gives a slower mechanical response. Both motors have advantages in certain applications. The specific application usually determines the type and size of the stepper motor required.

Basic Drives

The purpose of the drive is to get the correct voltage and current into the motor within a short time period and in an efficient manner. The direction of the current in the windings of the permanent magnet motors is important, as is the proper timing of motor excitation.

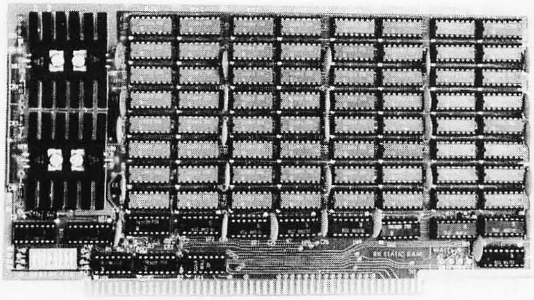
Figure 5 is a simplified diagram of one stepper motor winding, representing the motor winding as an inductor. The switches can alternately connect the winding to a plus and minus voltage supply. This results in a directional change in the current (and therefore the magnetic polarity) in the winding. This is a bipolar configuration. Notice that this requires two supplies in order to operate.

By using more switches, we can eliminate one supply, as shown in figure 6. This is commonly called the H drive or bridge drive. By turning on one opposite pair at a time, the winding leads are switched back and forth from ground to the supply. This achieves the desired result of changing the current direction in the winding. Care must be taken in both these drives to be sure that the switches are not turned on at the wrong time or they will short out the power supply (not to mention the rest of the system).

A bifilar motor, however, does not have this problem, because there are two windings on each pole. A drive configuration for a bifilar motor winding is shown in figure 7. Each pole has the windings connected so

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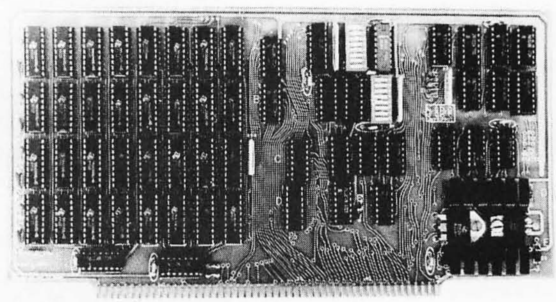


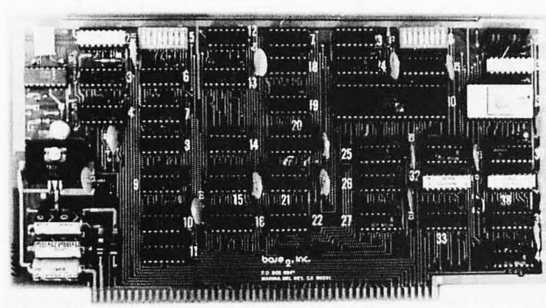
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This 8K board is available in two versions. The 8KS-B operates at 450ns for use with 8080 and 8080A microprocessor systems and Z-80 systems operating at 2MHz. The 8KS-Z operates at 250ns and is suitable for use with Z-80 systems operating at 4MHz. Both kits feature factory fresh 2102's (low power on 8KS-B) and includes sockets for all IC's. Support logic is low power Schottky to minimize power consumption. Address and data lines are fully buffered and 4K bank addressing is DIP switch selectable. Memory Protect/Unprotect, selectable wait states and battery backup are also designed into the board. Circuit boards are solder masked and silk-screened for ease of construction. These kits are the best memory value on the market! Available from stock . . . **8KS-B $125** (assembled and tested add $25.00)
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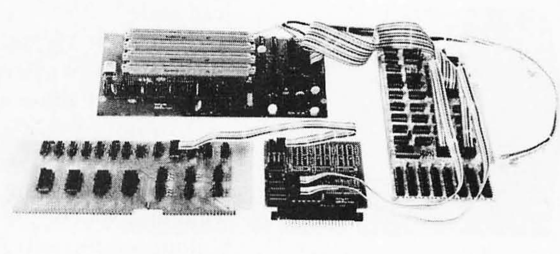


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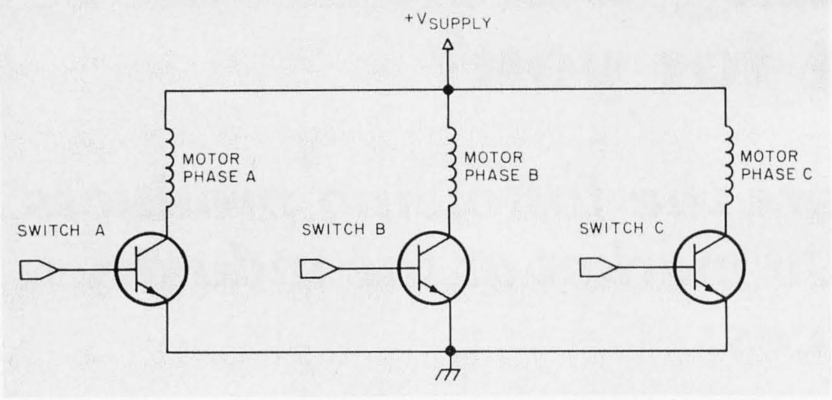


Figure 8: Drive scheme for a 3 phase variable reluctance stepper motor. Since there is no permanent magnet inside, only one power supply is needed.

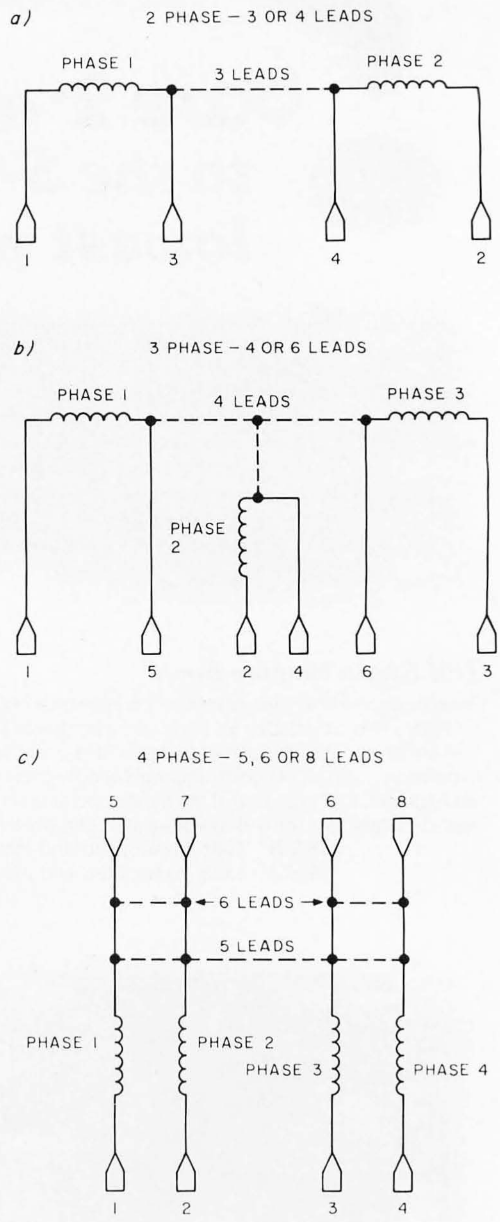


Figure 9: Connection diagrams for various motors. The dotted line in each configuration is an internal connection when less than the maximum number of leads are brought out. The number of leads brought out of the motor gives an approximate idea of the number of phases it has. By using an ohmmeter and measuring the difference between leads, the exact connection between phases of the motor can be found. If the motor is powered up and does not run correctly, reversing the leads of one of the phases should correct the problem (ie: in a 6 lead motor, exchange wires on terminals 3 and 4). The best thing to do if you are not sure of the wiring is to get the manufacturer's literature on the exact motor in question.

that current in one winding creates an opposite polarity on the pole from the other winding. The switches now decide which winding will be energized. The net effect is the same as the bipolar drives above, but only one supply is required, and the switching transistors (or motor) will not be damaged if they are accidentally turned on at the same time. On the other hand, the bipolar drives can give higher torque at lower speeds than the bifilar drives. Depending on which winding leads are available, the bifilar motor may also be connected to a bipolar type drive.

The variable reluctance motor does not depend on the direction of current flow since there is no magnet inside. Therefore it can use a drive scheme like the one in figure 8. Remember, however, that the variable reluctance motor does not have any holding power when de-energized. A connection diagram for several standard wiring configurations is shown in figures 9a, 9b and 9c. Figure 9a is a standard 3 or 4 lead bipolar stepper. Figures 9b and 9c are standard 4, 5, 6 and 8 lead motors. The only difference between the various types is that the common leads on the 6 and 8 lead types are connected internally on the 4 and 5 lead style.

A straight voltage supply drive for a bifilar step motor system is shown in figure 10. This type of drive exhibits some difficulty in forcing current into the windings. The inherent problem with this circuit is that there is a long time constant in the motor windings which prevents any quick, large buildup of current. As a result, little torque is produced. This can be improved, resulting in a common, fairly inexpensive stepper drive called the series resistance limiting drive (figure 11).

In figure 11, a resistor is inserted in series with the motor common leads, and the supply voltage is increased. A general rule

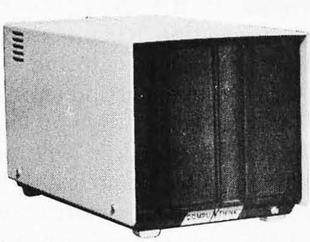
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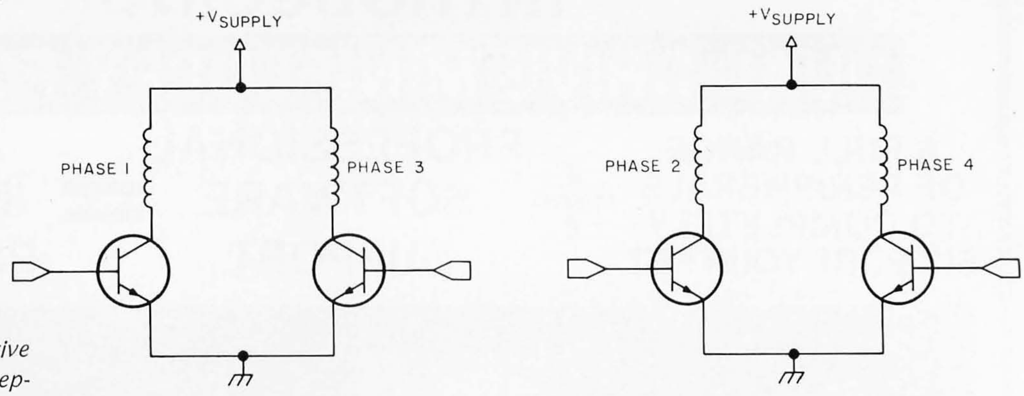


Figure 10: Simple drive for a 4 phase bifilar stepping motor.

of thumb for this scheme is to make the supply voltage approximately 5 times the voltage of the motor. The resistor is picked to drop the increase in voltage of the drive. The reason for the superiority of this modification is that the addition of the resistor changes the motor's time constant, allowing current flow to increase faster in a given time period. In order to maintain the rated current, the supply voltage is increased. The biggest disadvantage of this type of drive is in the power loss in the series resistors, which makes it very inefficient.

Various schemes have been developed and are used to improve upon the design. Figure 12a shows a scheme that uses a transistor and diode to switch out a high voltage from the windings once current has built up sufficiently. Figure 12b shows a method similar to that of a switching regulator. An initial controlled pulse source independent of the motor switches power to an inductor. A second pulse that increases in frequency as the speed of the motor increases also controls the power switch. In this design, there is enough current at standstill to supply adequate current for static torque (power on, but motor and switches not running). As the speed of the motor increases, the voltage increases because of the faster switching pulses. This continues until the motor supply voltage reaches the main supply voltage. At these speeds, the impedance of the motor is much higher and it can withstand the higher voltage present on the windings.

Figure 12c is a more efficient but more expensive scheme known as a chopper drive. In this scheme a high voltage is applied to the winding and removed when the current sense circuit detects a predetermined current in the windings.

For the personal computer experimenter, the series resistance limiting supply should be adequate for most applications.

Once the type of drive to be used has been decided upon, the most important item to consider is the drive transistor switches and protection circuits around them. The motor coil appears to the driver switch as a series connected inductor and resistor. An inductor in a switching circuit will cause problems if not dealt with properly. The winding also complicates matters by generating back electromotive force (back EMF), or voltage, which opposes the motor power supply. Since the motors are usually high current, low impedance devices, the drives require several stages of amplification.

In selecting the transistor, other characteristics are also important. First of all, the transistor must handle the current rating

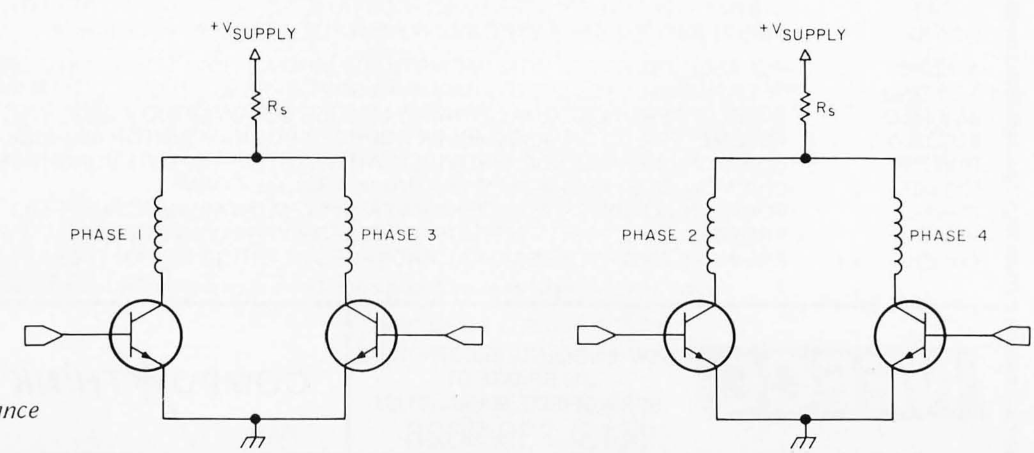
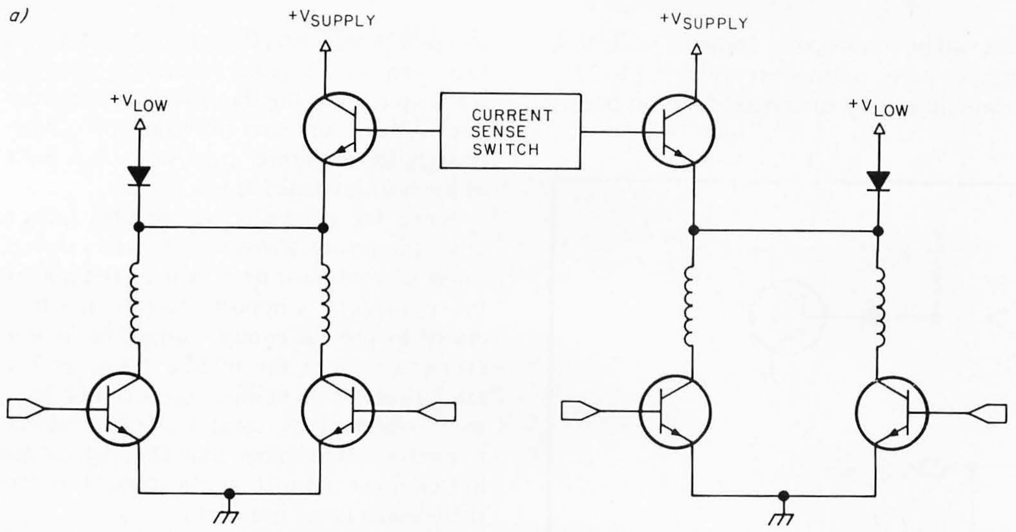
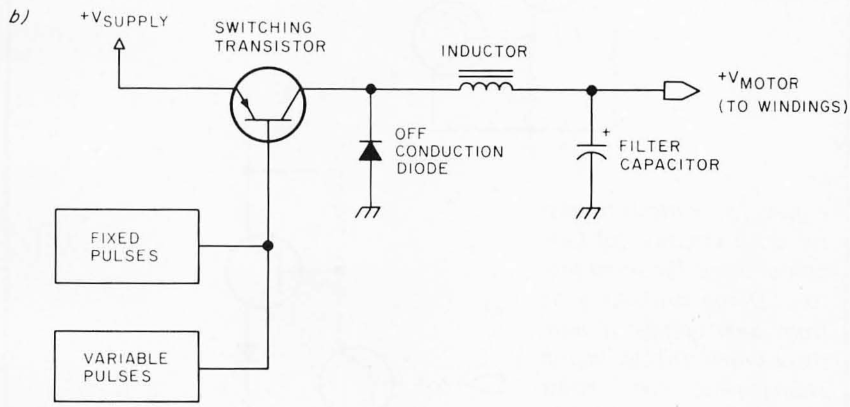


Figure 11: Series resistance limiting drive.





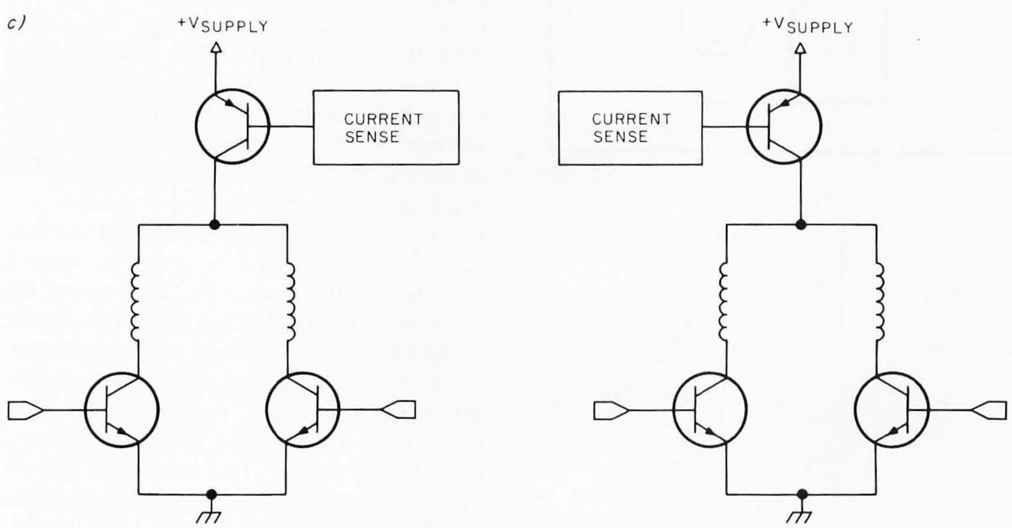


Figure 12: Three types of higher performance drives. (a) Dual voltage supply that turns off the high voltage supply when current is built up in the windings, leaving the low voltage supply on. (b) Switching regulator approach that increases the voltage to the windings as the motor speed increases, thus trying to keep the maximum current in the windings at any speed. (c) Chopper drive configuration which applies a high voltage to the windings to build up current quickly and then turns it off when a predetermined current is attained.

of the drive. Since the current rating of the motor is usually for 25°C and motor heating causes increased resistance, the transistor must be derated to take the heating of the motor into account. And they can get hot! The peak current seen in the transistor, which is about twice the average DC current, occurs when the coil phases are switched. A good rule is to not exceed 50 to 60 percent of the transistor's rating.

The next concern of the transistor is the reverse voltage rating of the collector-emitter and collector-base junctions. If the supply is 28 V, it doesn't mean that the rating of the transistor should be 28 V. Voltages in a bifilar motor winding, when switching, can peak at around 100 V with a 28 V supply, due to the transformer action of the windings.

Another concern of the transistor is the switching time. The longer the transistor takes to switch on or off, the more power

there will be to dissipate. Common switching times for power transistors are from 1 to 2 μs. A switching time of longer duration begins to waste power. An efficient switching transistor and an adequate protection network will help to keep the transistor's temperature down. Make sure that the heat sink is large enough for the power transistor, since most of the heat is created at low speeds.

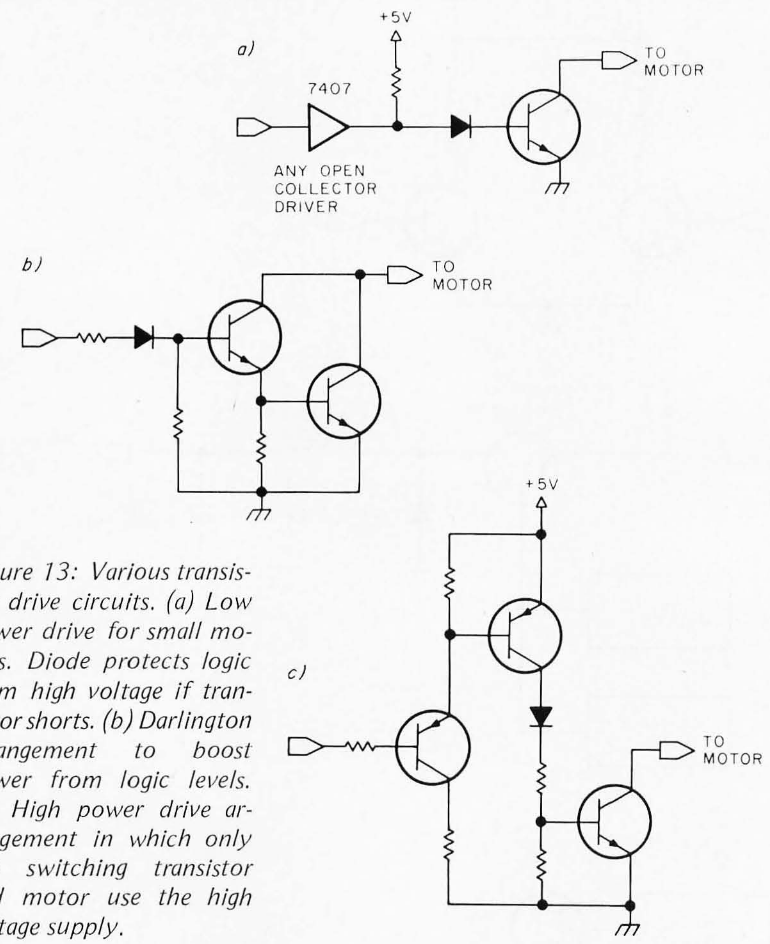


Figure 13: Various transistor drive circuits. (a) Low power drive for small motors. Diode protects logic from high voltage if transistor shorts. (b) Darlington arrangement to boost power from logic levels. (c) High power drive arrangement in which only the switching transistor and motor use the high voltage supply.

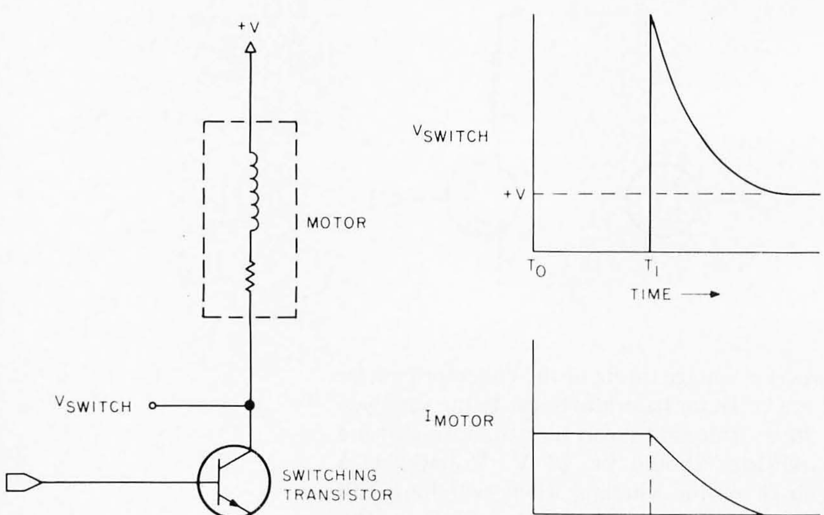


Figure 14: Switching transients in an unprotected winding. When the switch tries to open at time T1, the motor winding forces the voltage high so that it can maintain the same current.

Since the computer output port cannot drive the power transistors directly, several stages of gain must be provided. The gain of the transistors is important since it is necessary to provide enough current for motor rating, yet keep the middle stages in low saturation. The amplifier stages can be kept to a minimum by using Darlington power transistors. Remember that Darlingtons get hotter than normal power transistors, so they need a larger heat sink.

Table 1 gives a rough comparison of transistors available on the market that are suitable for stepper motor applications. Drive schemes for several different power levels are shown in figure 13. They all provide isolation between the processor interface and motor windings. The first is a low power drive for small motors. The second is a higher power drive that uses two discrete transistors in a Darlington configuration. The third technique utilizes the +5 V supply for the switching section and uses the motor supply only for the motor and output transistor.

Now that we have a method of getting power to the motor, we must be able to control the transient effects of the energy generated in the motor. The basic problem is shown in figure 14. Here, the switch (or transistor) has been on for some time and current is flowing through the winding. Suddenly, the switch is opened. Because the winding is an inductor, the current will continue to flow for some time and the voltage will instantly rise in order to keep it flowing at that rate. At this point the transient could easily knock out a transistor.

As figures 15a, 15b and 15c demonstrate, there are many ways to avoid this problem. The simplest method, shown in figure 15a, is to connect a diode from the winding back to the supply. This causes the current in the inductor to flow back around to the supply and eventually die out. The voltage across the switch at maximum would be only one diode voltage drop above the supply voltage. Figure 15b follows the same idea, but a resistor is added to the diode path. This allows a large voltage spike upon turnoff, but current flowing in the winding decays more rapidly. This is advantageous when running at higher speeds. A third arrangement (figure 15c) uses a zener diode in place of the resistor, limiting the voltage peak to a level approximately the same as that of the supply voltage plus the zener

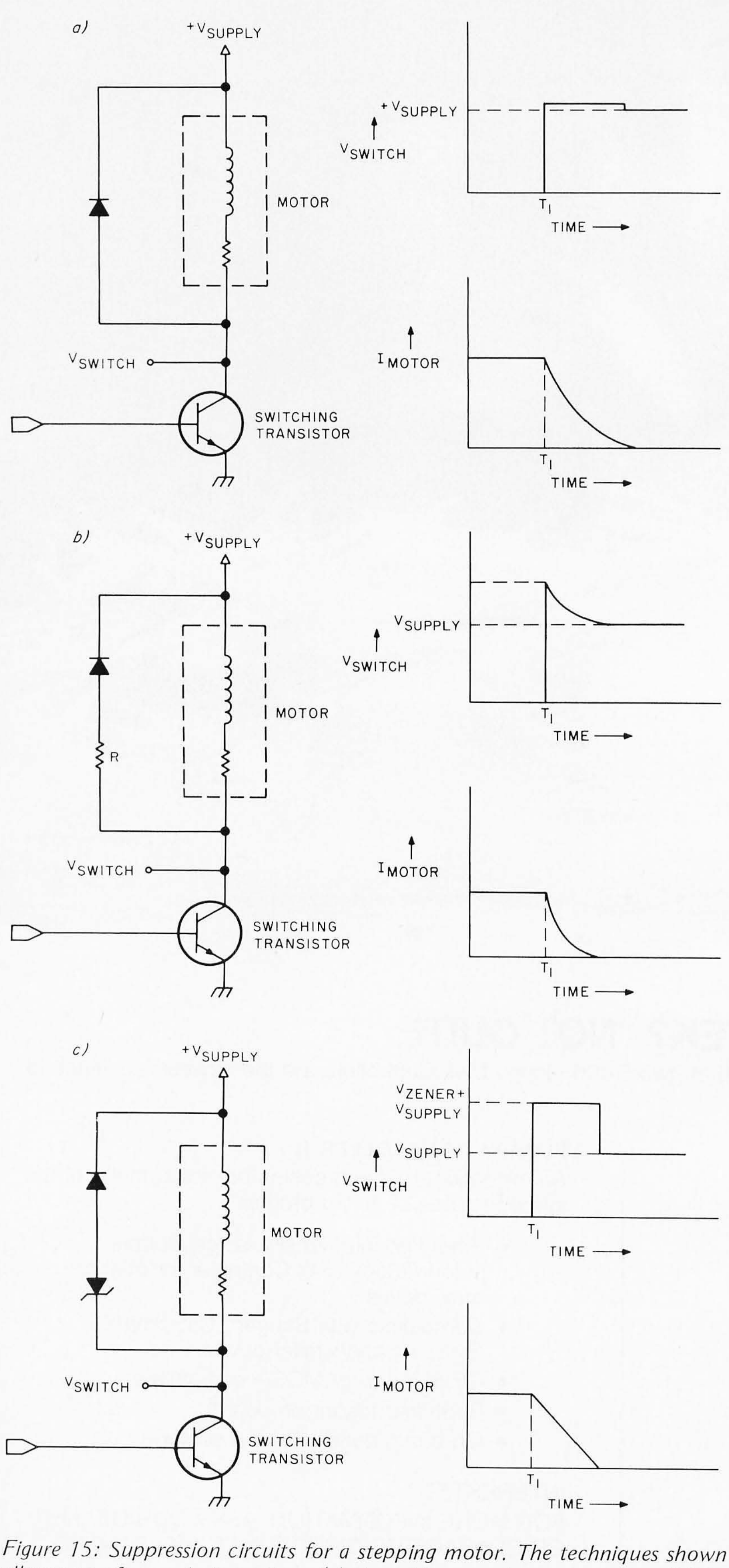


Figure 15: Suppression circuits for a stepping motor. The techniques shown allow one of several alternatives. (a) Use of lower voltage transistors. (b) Increase of motor performance. (c) A combination of both.

voltage. The rate of current decay is linear in this case and is still faster than the straight diode.

Another type of suppression circuit for bifilar motors is shown in figure 16. In this case, the other winding of the pole is used like a transformer to discharge the current. As an example, let's say that the motor is carrying 5 A and transistor Q1 shuts off. In order to keep current flowing in the windings, the motor finds a path from diode D1 through the other winding and back to the power supply. But what does this do to the voltages? First of all, the winding connected to diode D1 would be at −1 V. If there were 5 A flowing, the motor common would be at +45 V to cause 5 A to flow through the 4 Ω series resistor. On the other hand, the voltage across Q1 goes up to +95 V because the windings are acting like a center-tapped transformer. The same thing happens in the other winding when Q2 is turned off.

Part 2 of this article will describe techniques for interfacing stepper motors to personal computers.■

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4. "Use Stepper Motors in Motion-Control Applications," *EDN,* volume 23, number 14, August 5 1978, page 89.

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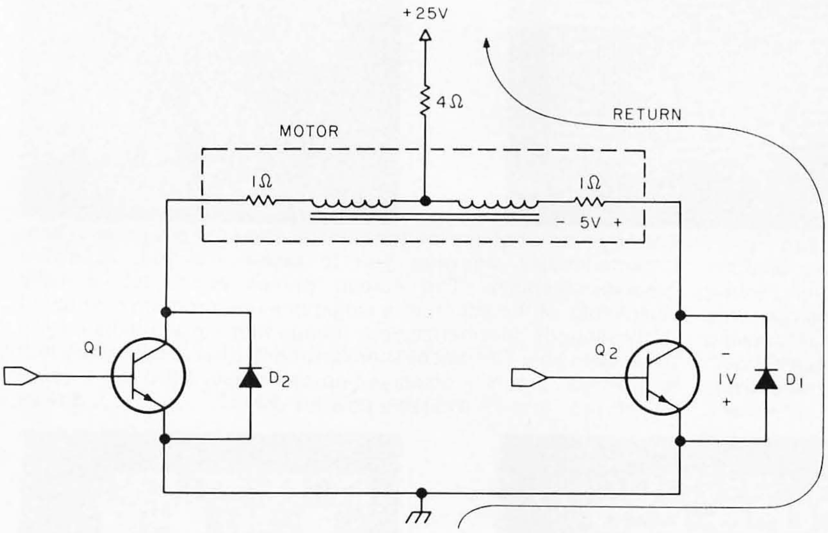


Figure 16: Suppression circuit for bifilar motor. This technique uses the off winding in the bifilar pair to continue the current flow as it decays. For example, assume that transistor Q1 shuts off. The arrow shows the path of current flow. Diode D1 is forced to conduct, which puts the off lead at −1 V. Since the current in this example is 5 A, the voltage across the 4 Ω resistor must be 20 V. This voltage must be added to the +25 V of the supply because the current flows into it. Therefore, the motor common lead will be at +45 V. The motor at this point can be thought of as a center tapped transformer and so the voltage from one coil to the center tap is +51 V (−5 drop due to motor resistance plus diode drop of −1 V). The total voltage across the transformer would then be +102 V because one end of the transformer is at −6 V.

Low Power

Device	I_c	BV_{ceo}	Gain	Power	Type	Case Type
T15135	0.5 A	50 V	20	0.7 W	NPN	To −92
2N2222A	0.5 A	40 V	10	0.5 W	NPN	To −5
2N2907A	0.5 A	60 V	50	0.4 W	PNP	To −18

Medium Power

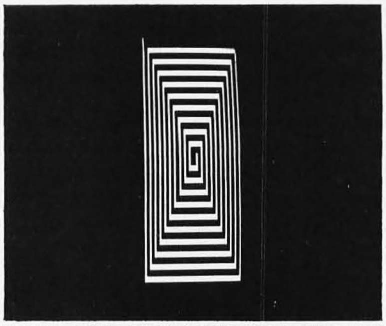
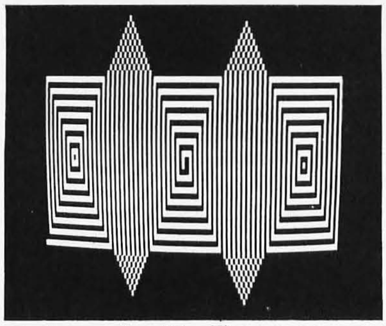
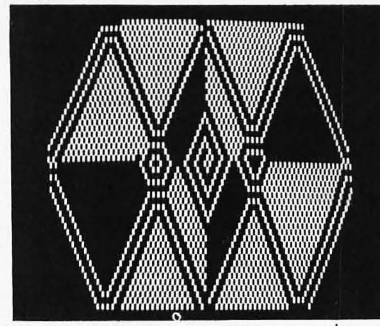
Device	I_c	BV_{ceo}	Gain	Power	Type	Case Type
2N3054	4.0 A	55 V	25	40 W	NPN	To −66
MJE13002	1.5 A	300 V	5	20 W	NPN	To −3
D45C5	4.0 A	45 V	10	30 W	PNP	To −229
TIP29C	1.0 A	100 V	20	2 W	NPN	To −229

High Power

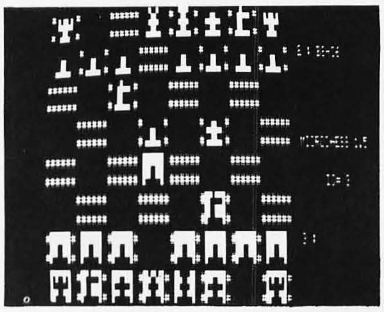
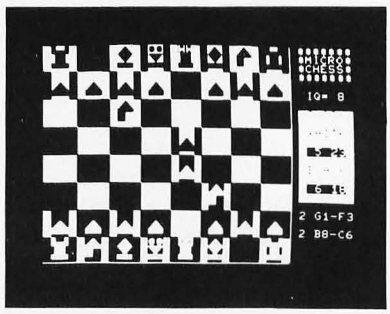
Device	I_c	BV_{ceo}	Gain	Power	Type	Case Type
TIP125	5 A	60 V	500	2 W	PNP	Darlington
2N3055	10 A	60 V	5	60 W	NPN	To −3
2N6056	8 A	80 V	750	70 W	NPN	Darlington
2N678B	15 A	60 V	50	30 W	PNP	Germanium
D56W1	5 A	200 V	3	70 W	NPN	GE To −3
2N3715	10 A	60 V	10	100 W	NPN	To −3
2N3716	10 A	80 V	10	100 W	NPN	To −3
TIP122	5 A	100 V	1000@3A	65 W	NPN	Darlington
TIP142	10 A	100 V	1000@5A	125 W	NPN	Darlington
TIP34C	10 A	100 V	20@3A	60 W	PNP	To −3

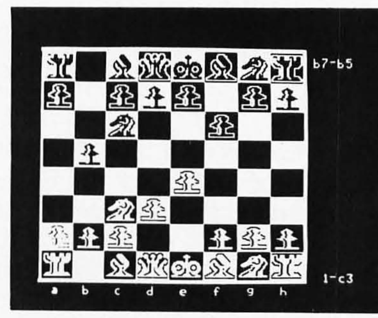
Table 1: Comparison of several transistors suitable for stepping motors. The transistors are available from most surplus electronics dealers.

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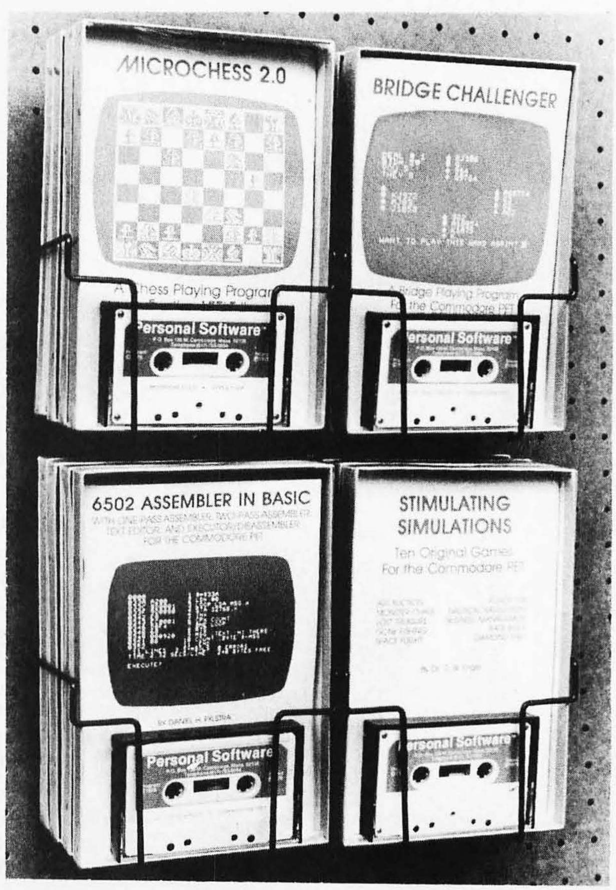
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Fast Fourier for the 6800

Richard H Lord
Bennett Rd
Durham NH 03824

If you're involved with music or speech processing applications with your computer, you've probably wished you could look at the frequency spectrum of your sampled signals. This may not be as difficult as you might guess, because here is a simple, straightforward fast Fourier transform (FFT) subroutine that can do the trick in just a few seconds.

A Microhistory of the Fast Fourier Transform

The analysis of waveforms for harmonic content has a long and fascinating history. Bernoulli and Euler developed the mathematics of the transform while experimenting with musical strings in 1728, nearly a hundred years before Jean Baptiste Fourier gave his name to the equations. Interest in prediction of the tides led Lord Kelvin to build a mechanical harmonic synthesizer that inspired the construction of increasingly complex mechanical harmonic analyzing machines. This trend culminated in the Mader-Ott machine of 1931, which is on display at the Smithsonian Institute in Washington DC.

With the growth of the telephone and the communication industry came sampling theory and the *discrete Fourier transform*. At first, discrete Fourier transforms were hand calculated and tabular forms called "schedules" were soon employed to speed the process. With the development of digital computers in the 1940s this task became somewhat easier to perform. The number of calculations required still made the concept of real time discrete Fourier transforms unlikely even on the ever faster new computers.

Then in the 1960s a number of matrix theory mathematicians, including J W Cooley and J W Tukey, went back to the "schedules" and discovered that a great many of the terms were redundant and could be factored out. The procedure they evolved became known as the *fast Fourier transform*, which reduces the number of calculations to the point that special hardware can be built to perform the transform in real time and display the frequency spectrum continuously on a video display.

The Basic Concepts

A number of books have been published describing the mathematics of the fast Fourier transform in some detail. A few of these contain sample programs in FORTRAN, ALGOL, or BASIC. However, the use of a high level language to perform this computation not only costs a great deal in speed and efficiency, but also obscures the simple binary processes that characterize the algorithm. Since high level languages do not usually support bit manipulation, these processes can become almost as time consuming as the arithmetic.

Clearly, assembly language programming of the fast Fourier transform offers many advantages, but the literature seldom provides any examples of assembly level code to illustrate how the equations are implemented. Thus the program described in this article may well be the reinvention of someone else's "wheel."

The details of the inner workings of the fast Fourier transforms are left to the technical references, but the basic concepts are not difficult to grasp. The transform involves complex products which behave in the manner of the coordinates of a rotating vector. When this vector is at angles which are multiples of 90 degrees, the sine and cosine terms of the equations become +1, 0, or −1. Since terms containing these values do not require computed multiplication, the arithmetic becomes very simple. Other terms cancel each other out in order to simplify the equations at other angles. By factoring these terms out of the transform, many unnecessary calculations may be eliminated.

The input data may be thought of as elements of an input matrix which will be multiplied by a transform matrix. The product is a matrix containing the transformed data. The redundant elements may be factored out of the transform matrix, converting it to the product of a number of simpler transforms. For an input array of 256 points, a discrete Fourier transform would require 256 by 256 complex products or 262,144 binary multiplications. The fast Fourier transform reduces this to eight simpler trans-

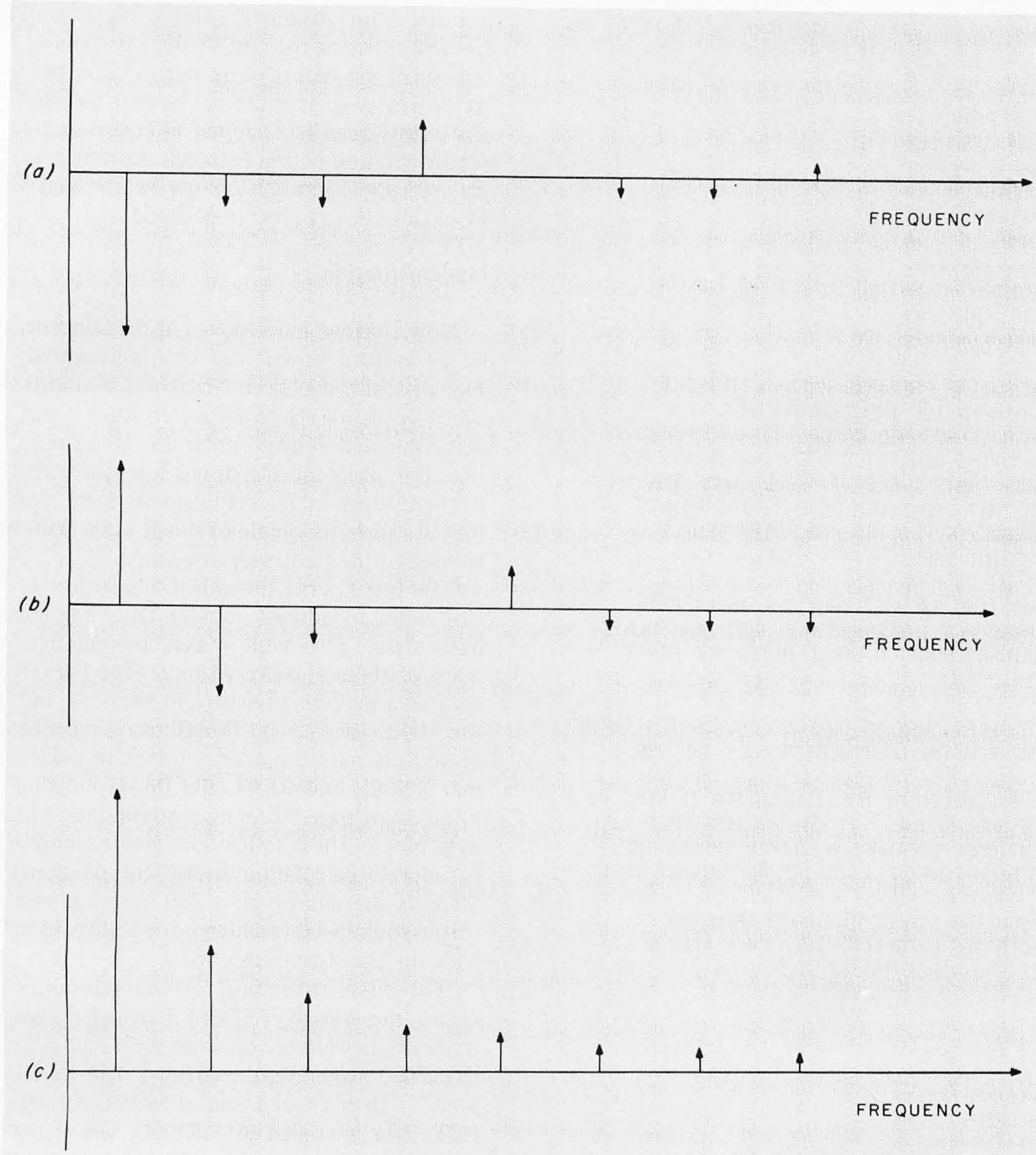


Figure 1: Fast Fourier transform of a square wave using the author's technique. The real (or sine) part of the transform is shown in (a). The imaginary (or cosine) part of the transform is shown in (b). The resulting transform is at (c). The resulting transform values are normally found by taking the square root of the sum of the squares of the cosine and sine elements. In order to save computational time, however, the author takes the sum of the absolute values of the terms, which introduces slight errors into the relative magnitudes of the components.

forms and ultimately requires 8 by 2 by 256 complex products, or 16,384 binary multiplications (1/16 the number of previous multiplications). Even greater savings are realized as the number of points increases.

Each of the simplified transforms operates on the data in pairs of complex points. The real and imaginary parts of a pair are transformed and the new values placed back in the array so that the transform is performed "in place." The algorithm then moves on to the next pair until all pairs have been transformed. The process is repeated for each of the eight stages of our 256 point transform, but on each pass the distance between pairs is changed.

On the first pass, adjacent points are paired. After completing a pair the algorithm skips down to the next. In a sense, the data has been split into 128 adjacent 2 point transforms. These 128 groups are known as cells. On each subsequent pass the distance between elements of the pair is doubled. In the second pass there are 64 cells, each four elements wide. On the final pass there is only one cell containing all 256 elements.

This process of forming pairs and cells causes the elements of the array to become scrambled. On the final pass the data is completely mixed up and must be sorted out before it can be used. The way it is scrambled is very interesting, though. If each element is assigned a binary number that represents its location in the array, the scrambled data makes it appear that the computer has read this binary address backwards. It is as if the binary word were swapped end for end so the most significant bit (MSB) appears where the least significant bit (LSB) should be.

This rearrangement of the data may be corrected by swapping each data point with its bit reverse addressed mate. The procedure

Listing 1: Routine in 6800 assembly language to perform a 256 point fast Fourier transform.

```
                        NAM    FFT#2
                        OPT    O,S,NOGEN
                 *********************
                 **  FAST FOURIER    **
                 **    TRANSFORM     **
                 **   SUBROUTINE     **
                 *********************
                 **   BY R.H. LORD   **
                 **  21 APRIL, 1978  **
                 *********************
                 **
                 ** THIS SUBROUTINE PERFORMS A 256 POINT FFT
                 ** ON THE DATA IN THE INPUT DATA TABLE.
                 ** INPUT DATA IS ASSUMED TO BE TWO'S COMPLEMENT.
                 ** THE SUBROUTINE GENERATES A COSINE (REAL) AND SINE
                 ** (IMAGINARY) DATA TABLE AT "REAL" AND "IMAG"
                 ** THE RESULTANT TRANSFORM DATA IS 128 POINTS
                 ** SYMMETRICALLY REFLECTED ABOUT THE CENTER OF
                 ** THE 256 POINT TABLE.
                 **
                 ** THE SUBROUTINE ASSUMES THAT THE INPUT DATA
                 ** IS ALL REAL AND THEREFORE DOES NOT MANIPULATE
                 ** THE IMAGINARY PORTION UNTIL AFTER THE FIRST
                 ** PASS.
                 **
                 ** ALL DATA AREAS MUST BE ON PAGE BOUNDARIES (XX00)
                 ** SINCE THE ROUTINE MANIPULATES ONLY THE LSB'S.
                 **
                 ** THE TWO'S COMPLEMENT MULTIPLICATION IS KEPT AS A
                 ** SEPARATE SUBROUTINE.  IT MAY BE PERFORMED WITH
                 ** A CONVENTIONAL SOFTWARE MULTIPLY SUBROUTINE
                 ** OR WITH A HARDWARE MULTIPLIER FOR HIGHER SPEED.
                 **
                 ** THE SUBROUTINE SCALES THE DATA WHENEVER
                 ** IT ANTICIPATES OVERFLOW.  THE SCALE FACTOR
                 ** COUNT IS AVAILABLE IN "SCLFCT".
                 **
                 **
                 **
                 **
                 *********************
                 **    DATA AREAS    **
                 *********************
      0800       INPUT  EQU    $0800    INPUT DATA TABLE
      0500       REALT  EQU    $0500    "REAL" DATA TABLE
      0600       IMAGT  EQU    $0600    "IMAG" DATA TABLE
      0400       SINET  EQU    $0400    SINE LOOKUP TABLE
                 *********************
0020                    ORG    $0020
                 *********************
                 **  BASE PAGE PTRS  **
                 *********************
0020 0002        RLPT1  RMB    2        "REAL" DATA POINTERS
0022 0002        RLPT2  RMB    2
0024 0002        IMPT1  RMB    2        "IMAG." DATA POINTERS
0026 0002        IMPT2  RMB    2
0028 0002        SINPT  RMB    2        SINE TABLE POINTER
002A 0001        CELNUM RMB    1        CELLS FOR THIS PASS
002B 0001        CELCT  RMB    1        CELL COUNTER FOR PASS
002C 0001        PAIRNM RMB    1        PAIRS/CELL
002D 0001        CELDIS RMB    1        CELL OFFSET(DISTANCE)
002E 0001        DELTA  RMB    1        ANGLE INCREMENT
002F 0001        SCLFCT RMB    1        SCALE FACTOR CTR.
0030 0001        COSA   RMB    1        TEMPORARY COSINE
0031 0001        SINA   RMB    1        TEMPORARY SINE
0032 0001        TREAL  RMB    1        TEMP.  REAL DATA
0033 0001        TIMAG  RMB    1        TEMP.  IMAG DATA
0034 0001        MSBY   RMB    1        MULTIPLY MSB
0035 0001        LSBY   RMB    1        MULTIPLY LSB
0036 0004        MPA    RMB    4        SOFTWARE MPY ACCUM.
                 ****************************
```

is called "bit swapping" and may be performed either at the end of the fast Fourier transform or before it is begun. The pretransform swap is more convenient because less points need be swapped and because the vector rotation within each cell is simpler. In the posttransform version the vector angles would also have to be bit swapped.

Implementation

Now that we have looked at the concept, let us look at how it can be implemented. The algorithm has been written as a subroutine (see listing 1) to be called by a signal gathering and display program. It assumes that this program has stored some time dependent data in 2's complement form and that a 256 byte sample of this is to be transformed to the frequency domain.

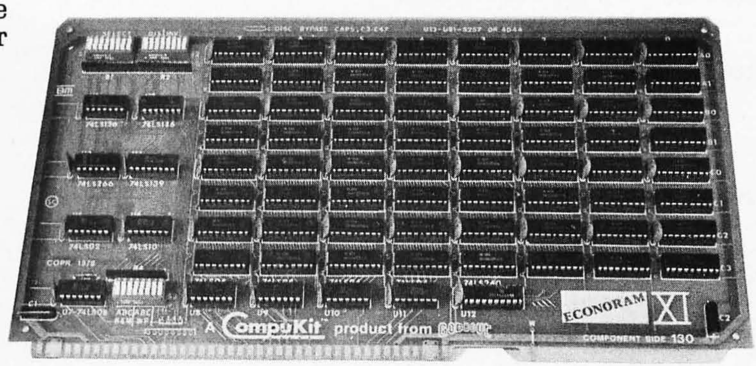
The fast Fourier transform subroutine begins with an address lookup table for the data areas. This table makes the reassignment of these areas very simple. The INPUT data area may be anywhere in memory, but the SINE, REAL, and IMAG arrays must be at address page boundaries (ie: at hexadecimal XX00), and REAL and IMAG must be in adjacent pages forming a continuous 512 byte block. These restrictions greatly simplify address calculation within the program. SINE is the address of a 256 byte sine and cosine lookup table which must be loaded in with the transform subroutine.

The first instruction of the subroutine clears the variable SCLFCT which keeps track of the number of times the data has to be scaled to prevent overflow. The IMAG array is then cleared and at MOVE the INPUT data is copied into REAL, where the transform will take place. The data is then prescrambled to put it in bit reverse order for the transform process. The bit reversed address is calculated by rotating the least significant bit of the address into the carry and rotating the reversed address out in the opposite direction. The new address is compared with the first address to prevent swapping the data back to the original order, then the two array elements are exchanged.

Once the swapping is complete, the data is ready to be transformed. The fast Fourier transform is performed in eight separate passes; before each pass begins, the data is tested by SCALE to prevent any overflow. For the first pass there are 128 cells formed by adjacent pairs of data. In this pass the vector angle steps in multiples of 180 degrees. This means that all the sine terms are 0 and the cosine terms are either +1 or −1. Also there is no data yet in the IMAG array. The general equations thus become greatly simplified and the pass is reduced to addition and subtraction among elements of the

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Listing 1, continued:

```
                      **  START OF TRANSFORM      **
                      *****************************
0200                          ORG    $0200
0200 20 08                    BRA    START    JUMP AROUND PARAMETERS
                      *****************************
                      **  ADDRESS LOOK-UP TABLE  **
                      **    FOR DATA AREAS       **
                      *****************************
0202 0800             INPD    FDB    INPUT    SET UP DATA AREAS
0204 0500             REAL    FDB    REALT
0206 0600             IMAG    FDB    IMAGT
0208 0400             SINE    FDB    SINET
                      *****************************
                      **
020A 7F 002F          START   CLR    SCLFCT   NOTHING SCALED YET
                      **
                      *****************************
                      **    INPUT DATA SET-UP    **
                      *****************************
020D FE 0206          CLEAR   LDX    IMAG     CLEAR OUT IMAG.
0210 5F                       CLR B           SET UP COUNTER
0211 6F 00            CLR1    CLR    0,X      CLEAR MEMORY
0213 08                       INX
0214 5A                       DEC B
0215 26 FA                    BNE    CLR1
0217 FE 0202          MOVE    LDX    INPD     SET UP POINTERS
021A DF 20                    STX    RLPT1
021C FE 0204                  LDX    REAL
021F DF 22                    STX    RLPT2
0221 DE 20            MOV1    LDX    RLPT1    MOVE INPUT DATA
0223 A6 00                    LDA A  0,X      TO "REAL" ARRAY
0225 08                       INX
0226 DF 20                    STX    RLPT1
0228 DE 22                    LDX    RLPT2
022A A7 00                    STA A  0,X
022C 7C 0023                  INC    RLPT2+1
022F 26 F0                    BNE    MOV1     TEST PAGE OVERFLOW
                      *****************************
                      **  PRE-TRANSFORM BIT SWAP **
                      *****************************
0231 FE 0204                  LDX    REAL     SET UP DATA POINTERS
0234 DF 20                    STX    RLPT1
0236 DF 22                    STX    RLPT2
0238 C6 08            BITREV  LDA B  #8       SET BIT COUNTER
023A 96 21                    LDA A  RLPT1+1  GET POINTER 1
023C 46               BRV1    ROR A           REVERSE BIT ORDER
023D 79 0023                  ROL    RLPT2+1  FOR SECOND POINTER
0240 5A                       DEC B           COUNT BITS
0241 26 F9                    BNE    BRV1
0243 96 23                    LDA A  RLPT2+1  GET REVERSED BYTE
0245 91 21                    CMP A  RLPT1+1  COMPARE WITH #1
0247 25 0E                    BCS    SWP1     BRANCH IF ALREADY SWAPPED
0249 DE 20            SWAP    LDX    RLPT1    GET POINTER 1
024B A6 00                    LDA A  0,X      GET VAL 1
024D DE 22                    LDX    RLPT2    GET POINTER 2
024F E6 00                    LDA B  0,X      GET VAL 2
0251 A7 00                    STA A  0,X      REPLACE WITH VAL 1
0253 DE 20                    LDX    RLPT1    GET FIRST POINTER
0255 E7 00                    STA B  0,X      COMPLETE SWAP
0257 7C 0021          SWP1    INC    RLPT1+1  DO NEXT POINT PAIR
025A 26 DC                    BNE    BITREV   UNLESS ALL ARE DONE
                      *************************************
                      **       FFT  FIRST PASS           **
                      *************************************
                      **  SINCE IN PASS 1 ALL ANGLES     **
                      **    ARE MULTIPLES OF 180 DEG.    **
                      **  THERE ARE NO PRODUCT TERMS.    **
                      **    AND NO IMAGINARY TERMS YET   **
                      **  HENCE A FAST VERSION OF PASS 1 **
                      *************************************
025C BD 0333          PASS1   JSR    SCALE    SCALE IF ANY OVER-RANGE DATA
```

REAL array. Considerable time is saved by making this pass separate and bypassing the unneeded table lookup and multiply routines.

Once this pass is completed, the arithmetic gets much more complex. The remaining seven passes are performed by a general fast Fourier transform algorithm. It begins at FPASS by setting up 64 cells of four elements with the pairs separated by two units. The vector angle is set to increment by 90 degrees by setting DELTA to 64. At NPASS the pointers are set up for the first cell and the pass then begins with a sine and cosine table lookup. The complex data pair is then processed using the standard fast Fourier transform equations:

$$TR = RN\,COS(w) + IN\,SIN(w)$$
$$TI = IN\,COS(w) - RN\,SIN(w)$$

$$RM' = RM + TR \qquad RN' = RM - TR$$
$$IM' = IM + TI \qquad IN' = IM - TI$$

After each pair has been transformed the angle is incremented by DELTA and the next pair processed. When all pairs in a cell have been transformed the routine moves down to the next cell and returns to NCELL to continue the process. When the last cell has been done, CELCT becomes 0 and the pass is complete.

At the end of each pass the number of cells and the angle increment are divided in half and the pair separation and number of pairs per cell are doubled. The whole process is then repeated by branching to NPASS until the end of the last pass when the number of cells becomes 0. The routine then branches to DONE and returns to the calling program.

The SCALE subroutine is used to anticipate and prevent overflow of the 8 bit data. It is called before each pass and begins by testing the value of each data point. If any point exceeds the range of -64 to +64 the subroutine branches to SCL4 where the entire array is scaled down by a factor of 2. The variable SCLFCT is incremented to indicate the total number of times the data has been scaled.

The multiply routine has been placed at the end of the program to make substitution of other versions easy. The original program was written for a hardware multiplier similar to the device described by Bryant and Swasdee in April 1978 BYTE, page 28. To eliminate the need for such exotic hardware, a software multiply routine has been substituted with some increase in transform time. After the multiplication is completed

Listing 1, continued:

```
025F FE 0204         LDX    REAL      SET UP POINTERS
0262 DF 20           STX    RLPT1
0264 DE 20     PA1   LDX    RLPT1     GET POINTER
0266 A6 00           LDA A  0,X       GET RM
0268 E6 01           LDA B  1,X       AND RN
026A 36              PSH A            SAVE RM
026B 1B              ABA              RM'=RM+RN
026C A7 00           STA A  0,X       STORE NEW RM'
026E 32              PUL A            GET OLD RM
026F 10              SBA              RN'=RM-RN
0270 A7 01           STA A  1,X       STORE RN'
0272 7C 0021         INC    RLPT1+1   MOVE TO NEXT PAIR
0275 7C 0021         INC    RLPT1+1
0278 26 EA           BNE    PA1       KEEP GOING TILL DONE
               ********************************
               **  COMPUTATION OF FFT        **
               **      PASS 2 THRU N         **
               ********************************
027A 86 40     FPASS LDA A  #64       SET UP PARAMETERS
027C 97 2A           STA A  CELNUM    FOR CELL COUNT
027E 97 2E           STA A  DELTA     AND ANGLE
0280 86 02           LDA A  #2        AND FOR
0282 97 2C           STA A  PAIRNM    PAIRS/CELL
0284 97 2D           STA A  CELDIS    DISTANCE BETWEEN PAIRS
0286 BD 0333 NPASS   JSR    SCALE     KEEP DATA IN RANGE
0289 96 2A           LDA A  CELNUM    GET NUMBER OF CELLS
028B 97 2B           STA A  CELCT     PUT IN COUNTER
028D FE 0204         LDX    REAL      SET UP POINTERS
0290 DF 20           STX    RLPT1
0292 DF 22           STX    RLPT2
0294 FE 0206         LDX    IMAG
0297 DF 24           STX    IMPT1
0299 DF 26           STX    IMPT2
029B FE 0208 NCELL   LDX    SINE
029E DF 28           STX    SINPT
02A0 D6 2C           LDA B  PAIRNM    GET PAIRS/CELL CTR.
02A2 96 21     NC1   LDA A  RLPT1+1   GET POINTER 1 LSBY
02A4 9B 2D           ADD A  CELDIS    ADD PAIR OFFSET
02A6 97 23           STA A  RLPT2+1   SET BOTH POINTER 2'S
02A8 97 27           STA A  IMPT2+1
02AA 37              PSH B            SAVE PAIR CTR
02AB DE 28           LDX    SINPT     SET UP SINE LOOKUP
02AD A6 00           LDA A  0,X       GET COSINE OF ANGLE
02AF 97 30           STA A  COSA      SAVE ON BASE PAGE
02B1 A6 40           LDA A  64,X      GET SINE
02B3 97 31           STA A  SINA      AND SAVE IT
02B5 DE 22           LDX    RLPT2     GET "REAL" POINTER 2
02B7 A6 00           LDA A  0,X       GET RN
02B9 36              PSH A            SAVE IT
02BA D6 30           LDA B  COSA      GET COSINE
02BC BD 036A         JSR    MPY       MAKE RN*COS(A)
02BF 97 32           STA A  TREAL     SAVE IT
02C1 32              PUL A            RESTORE RN
02C2 D6 31           LDA B  SINA      GET SINE
02C4 BD 036A         JSR    MPY       RN*SIN(A)
02C7 97 33           STA A  TIMAG
02C9 DE 26           LDX    IMPT2     GET IMAG. POINTER 2
02CB A6 00           LDA A  0,X       GET IN
02CD 36              PSH A            SAVE IT
02CE D6 31           LDA B  SINA      GET SINE
02D0 BD 036A         JSR    MPY       IN*SIN(A)
02D3 9B 32           ADD A  TREAL     TR=RN*COS+IN*SIN
02D5 97 32           STA A  TREAL
02D7 32              PUL A            RESTORE IN
02D8 D6 30           LDA B  COSA      GET COSINE
02DA BD 036A         JSR    MPY       IN*COS(A)
02DD 90 33           SUB A  TIMAG     TI=IN*COS-RN*SIN
02DF 97 33           STA A  TIMAG
02E1 DE 20           LDX    RLPT1
02E3 A6 00           LDA A  0,X       GET RM
02E5 16              TAB              SAVE IT
```

the data must be scaled up by a factor of 2. This is because the sine and cosine terms represent fractional binary values. The least significant bit is shifted in from the lower byte to preserve accuracy.

Analyzing the Results

After working with all this mathematics and software, what do you end up with? We started with a 256 point time domain sample in REAL. The fast Fourier transform converts this to a frequency domain sample corresponding to the spectrum of the input. The first element of each array represents the DC component of the input. The next element represents the sine wave with period equal to the duration of the input sample. Each remaining element depicts a multiple of this frequency until the middle of the array is reached, representing 128 cycles per period. The remainder of the array is symmetrical to the first 128 points.

Each element in the REAL and IMAG arrays represents information about one frequency component of the input sample. But why do we end up with two arrays, and what do the cosine terms of REAL and the sine terms of IMAG really mean to us? Usually this information is described in terms of amplitude and phase of the component, and often the phase information is of little interest. The cosine and sine terms represent the X and Y components of a vector with length and angle equal to the *amplitude and phase* terms that we are after. All we have to do is find the length of the vector from the square root of the sum of squares of the cosine and sine terms.

The only problem is that this calculation requires almost as much time as the transform, due to the square root. If we bypass the root and display the sum of squares (the power spectrum) we miss most of the detail of the lesser components. I have found that the highly unmathematical solution of displaying the sum of the absolute values is fairly satisfactory, although it introduces some error in the relative amplitude of peaks. This value is then sent to a digital to analog converter for display on an oscilloscope.

Putting the Fast Fourier Transform to Work

This program has a number of interesting applications for speech recognition, image processing, and the synthesis of musical instruments. A recent issue of *The Computer Music Journal* even describes a program for transcribing recordings back into sheet music (see bibliography, page 118).

Listing 1, continued:

```
0 2E6 9B 32             ADD A  TREAL    RM'=RM+TR
02E8 A7 00              STA A  0,X
02EA DE 22              LDX    RLPT2
02EC D0 32              SUB B  TREAL    RN'=RM-TR
02EE E7 00              STA B  0,X
02F0 DE 24              LDX    IMPT1
02F2 A6 00              LDA A  0,X      GET IM
02F4 16                 TAB             SAVE IT
02F5 9B 33              ADD A  TIMAG    IM'=IM+TI
02F7 A7 00              STA A  0,X
02F9 DE 26              LDX    IMPT2
02FB D0 33              SUB B  TIMAG    IN'=IM-TI
02FD E7 00              STA B  0,X
02FF 96 29              LDA A  SINPT+1  INCREMENT ANGLE
0301 9B 2E              ADD A  DELTA
0303 97 29              STA A  SINPT+1
0305 7C 0021            INC    RLPT1+1  INCREMENT POINTERS
0308 7C 0025            INC    IMPT1+1
030B 33                 PUL B           GET PAIR COUNTER
030C 5A                 DEC B           DECREMENT
030D 26 93              BNE    NC1      DO NEXT PAIR
030F 96 21              LDA A  RLPT1+1  GET POINTERS
0311 9B 2D              ADD A  CELDIS   ADD CELL OFFSET
0313 97 21              STA A  RLPT1+1
0315 97 25              STA A  IMPT1+1
0317 7A 002B            DEC    CELCT    DECR. CELL COUNTER
031A 27 03              BEQ    NP1      NEXT PASS?
031C 7E 029B            JMP    NCELL    NO, DO NEXT CELL
                   **
                   ** CHANGE PARAMETERS FOR NEXT PASS **
                   **
031F 74 002A NP1        LSR    CELNUM   HALF AS MANY CELLS
0322 27 0C              BEQ    DONE     NO MORE CELLS
0324 78 002C            ASL    PAIRNM   TWICE AS MANY PAIRS
0327 78 002D            ASL    CELDIS   TWICE AS FAR APART
032A 74 002E            LSR    DELTA    HALF THE ANGLE
032D 7E 0286            JMP    NPASS    DO NEXT PASS
                   *******************************
                   **  END OF FFT ROUTINE       **
                   *******************************
                   **
0330 39      DONE       RTS             EXIT FFT SUBROUTINE
0331 0002               RMB    2        ROOM FOR JUMP EXIT
                   **
                   ***************************
                   **  OVER-RANGE DATA SCALE **
                   ***************************
0333 FE 0204 SCALE      LDX    REAL     SET UP DATA POINTER
0336 5F                 CLR B           SET UP PAIR CTR
0337 37      SCL1       PSH B           SAVE PAIR CTR.
0338 C6 02              LDA B  #2       SET UP PAIR
033A A6 00   SCL2       LDA A  0,X      GET DATA
033C 08                 INX             BUMP POINTER
033D 81 C0              CMP A  #$C0     TEST LOWER LIMIT
033F 22 04              BHI    SCL3     SKIP TO NEXT POINT
0341 81 40              CMP A  #$40     TEST UPPER LIMIT
0343 24 08              BCC    SCL4     SCALE IF OUT OF RANGE
0345 5A      SCL3       DEC B           TEST NEXT POINT
0346 26 F2              BNE    SCL2
0348 33                 PUL B
0349 5A                 DEC B
034A 26 EB              BNE    SCL1
034C 39                 RTS             DONE TESTING
034D 33      SCL4       PUL B           RESTORE STACK
034E 7C 002F            INC    SCLFCT   BUMP SCALE FACTOR COUNT
0351 FE 0204            LDX    REAL     SET UP TABLE PTR.
0354 5F                 CLR B           SET UP PAIR CTR
0355 37      SCL5       PSH B           SAVE IT
0356 C6 02              LDA B  #2       SET UP PAIR
0358 A6 00   SCL6       LDA A  0,X      GET DATA
035A 8B 80              ADD A  #$80     MAKE IT ABSOLUTE
```

To get meaningful information from the transform, the input data must be sampled judiciously. While this program in theory is capable of analyzing 128 harmonics of a given sample, this is only true when the input represents exactly one complete cycle of the waveform being analyzed. Most data just doesn't come packaged that way.

To accurately measure the pitch of a sound you must sample many cycles. To analyze harmonics you want to sample few. The best result for real data will always be a compromise between range (bandwidth) and resolution. Both can be increased only by analyzing more points, which takes more time.

After experimenting with one sample at a time you will probably want to try continuous analysis. The input data pointer at hexadecimal address 0202 can be moved through an input buffer by the program that calls the transform. At roughly three seconds per transform, the data cannot suitably be analyzed in real time. A sample of a few seconds of data can be continuously analyzed and the changes slowly displayed. This is probably most easily accomplished by transferring the "sum of absolute value" data to a display buffer which is then scanned by an interrupt driven display program.

Bigger, Better, and Faster

Like most software, this program exists to be rewritten. No attempt was made to optimize execution speed. Preliminary experiments with an MMI-67558 hardware multiplier took slightly under one second. This relatively minor improvement was probably due to the time wasted in moving the data in and out of the multiplier. Perhaps it can be streamlined to the extent that a continuous display can be created. I plan to try a version for the 6502 microprocessor with hope of adding still more speed.

The algorithm is simple enough so that conversion should be easy. Enterprising 8080 and Z-80 enthusiasts shouldn't have too much trouble adapting the principles to their computers, either. Conversion to double precision or 512 to 1024 points should also be possible, although the present addressing scheme would have to be abandoned.

I hope this program will provide you with a tool that will be a lot of fun to play with. Please write and tell me what uses you find for it and any improvements you would like to suggest.

Continued on page 118

Listing 1, continued:

```
035C 44              LSR A            DIVIDE IT BY 2
035D 80 40           SUB A   #$40     MAKE IT 2'S COMP.
035F A7 00           STA A   0,X
0361 08              INX              BUMP POINTER
0362 5A              DEC B            NEXT POINT
0363 26 F3           BNE     SCL6
0365 33              PUL B
0366 5A              DEC B            NEXT PAIR
0367 26 EC           BNE     SCL5
0369 39              RTS              RETURN
                *******************************
                **  2'S COMP. MULTIPLY SUBR.  **
                *******************************
036A 97 37      MPY  STA A   MPA+1    STORE MULTIPLIER
036C D7 39           STA B   MPA+3    AND MULTIPLICAND
036E 4F              CLR A
036F 97 36           STA A   MPA      CLEAR MSB'S
0371 97 38           STA A   MPA+2
0373 97 34           STA A   MSBY     CLEAR PRODUCT
0375 97 35           STA A   LSBY
0377 5D              TST B
0378 2C 03           BGE     MPY1     NEGATIVE MULTIPLICAND ?
037A 73 0038         COM     MPA+2    EXTEND NEG TO MSB
037D 7D 0037    MPY1 TST     MPA+1
0380 2C 03           BGE     MPY2     NEG MULTIPLIER ?
0382 73 0036         COM     MPA      EXTEND NEG TO MSB
0385 C6 0F      MPY2 LDA B   #15      SET UP COUNTER
0387 77 0036    MPY3 ASR     MPA      SHIFT X RIGHT
038A 76 0037         ROR     MPA+1
038D 24 0C           BCC     MPY4     BIT WAS ZERO
038F 96 39           LDA A   MPA+3    ADD Y TO PRODUCT
0391 9B 35           ADD A   LSBY
0393 97 35           STA A   LSBY
0395 96 38           LDA A   MPA+2    MSB'S
0397 99 34           ADC A   MSBY
0399 97 34           STA A   MSBY
039B 78 0039    MPY4 ASL     MPA+3    SHIFT Y LEFT
039E 79 0038         ROL     MPA+2
03A1 5A              DEC B
03A2 26 E3           BNE     MPY3
                **
                ** SCALE IT UP **
                **
03A4 96 34           LDA A   MSBY
03A6 79 0035         ROL     LSBY
03A9 49              ROL A
                **
                ** RETURN WITH PRODUCT IN A
                **
03AA 39              RTS
                *******************************
                **     END OF FFT PROGRAM     **
                *******************************
                     END

    INPUT   0800   REALT   0500   IMAGT   0600   SINET   0400
    RLPT1   0020   RLPT2   0022   IMPT1   0024   IMPT2   0026
    SINPT   0028   CELNUM  002A   CELCT   002B   PAIRNM  002C
    CELDIS  002D   DELTA   002E   SCLFCT  002F   COSA    0030
    SINA    0031   TREAL   0032   TIMAG   0033   MSBY    0034
    LSBY    0035   MPA     0036   INPD    0202   REAL    0204
    IMAG    0206   SINE    0208   START   020A   CLEAR   020D
    CLR1    0211   MOVE    0217   MOV1    0221   BITREV  0238
    BRV1    023C   SWAP    0249   SWP1    0257   PASS1   025C
    PA1     0264   FPASS   027A   NPASS   0286   NCELL   029B
    NC1     02A2   NP1     031F   DONE    0330   SCALE   0333
    SCL1    0337   SCL2    033A   SCL3    0345   SCL4    034D
    SCL5    0355   SCL6    0358   MPY     036A   MPY1    037D
    MPY2    0385   MPY3    0387   MPY4    039B
TOTAL ERRORS 00000
```

Continued from page 117

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Listing 2: The object code listing in hexadecimal format of the assembly language program given in listing 1. This listing can be used to manually enter the program or as a confirmation copy for the PAPERBYTE^{tm} bar code representation given in figure 2. The format used for this listing is a 2 byte address field, followed by up to 16 bytes of data, with a 1 byte check digit at the end of each line. Note that the data in hexadecimal locations 0400 to 04FF constitute the sine and cosine lookup table which must be loaded with the transform subroutine.

```
0200 20 08 08 00 05 00 06 00 04 00 7F 00 2F FE 02 06   F3
0210 5F 6F 00 08 5A 26 FA FE 02 02 DF 20 FE 02 04 DF   34
0220 22 DE 20 A6 00 08 DF 20 DE 22 A7 00 7C 00 23 26   39
0230 F0 FE 02 04 DF 20 DF 22 C6 08 96 21 46 79 00 23   5B
0240 5A 26 F9 96 23 91 21 25 0E DE 20 A6 00 DE 22 E6   A1
0250 00 A7 00 DE 20 E7 00 7C 00 21 26 DC BD 03 33 FE   1C
0260 02 04 DF 20 DE 20 A6 00 E6 01 36 1B A7 00 32 10   CA
0270 A7 01 7C 00 21 7C 00 21 26 EA 86 40 97 2A 97 2E   3E
0280 86 02 97 2C 97 2D BD 03 33 96 2A 97 2B FE 02 04   88
0290 DF 20 DF 22 FE 02 06 DF 24 DF 26 FE 02 08 DF 28   1D
02A0 D6 2C 96 21 9B 2D 97 23 97 27 37 DE 28 A6 00 97   73
02B0 30 A6 40 97 31 DE 22 A6 00 36 D6 30 BD 03 6A 97   81
02C0 32 32 D6 31 BD 03 6A 97 33 DE 26 A6 00 36 D6 31   46
02D0 BD 03 6A 9B 32 97 32 32 D6 30 BD 03 6A 90 33 97   7C
02E0 33 DE 20 A6 00 16 9B 32 A7 00 DE 22 D0 32 E7 00   4A
02F0 DE 24 A6 00 16 9B 33 A7 00 DE 26 D0 33 E7 00 96   B7
0300 29 9B 2E 97 29 7C 00 21 7C 00 25 33 5A 26 93 96   CC
0310 21 9B 2D 97 21 97 25 7A 00 2B 27 03 7E 02 9B 74   BB
0320 00 2A 27 0C 78 00 2C 78 00 2D 74 00 2E 7E 02 86   4E
0330 39 00 00 FE 02 04 5F 37 C6 02 A6 00 08 81 C0 22   AC
0340 04 81 40 24 08 5A 26 F2 33 5A 26 EB 39 33 7C 00   E9
0350 2F FE 02 04 5F 37 C6 02 A6 00 8B 80 44 80 40 A7   ED
0360 00 08 5A 26 F3 33 5A 26 EC 39 97 37 D7 39 4F 97   17
0370 36 97 38 97 34 97 35 5D 2C 03 73 00 38 7D 00 37   87
0380 2C 03 73 00 36 C6 0F 77 00 36 76 00 37 24 0C 96   CD
0390 39 9B 35 97 35 96 38 99 34 97 34 78 00 39 79 00   65
03A0 38 5A 26 E3 96 34 79 00 35 49 39                  95

0400 7F 7F 7F 7F 7F 7F 7E 7E 7D 7D 7C 7B 7A 79 78 77   C9
0410 76 75 73 72 71 6F 6D 6C 6A 68 66 65 63 61 5E 5C   A4
0420 5A 58 56 53 51 4E 4C 49 47 44 41 3F 3C 39 36 33   78
0430 31 2E 2B 28 25 22 1F 1C 19 16 12 0F 0C 09 06 03   A2
0440 00 FD FA F7 F4 F1 EE EA E7 E4 E1 DE DB D8 D5 D2   8F
0450 CF CD CA C7 C4 C1 BF BC B9 B7 B4 B2 AF AD AA A8   B1
0460 A6 A4 A2 9F 9D 9B 9A 98 96 94 93 91 8F 8E 8D 8B   78
0470 8A 89 88 87 86 85 84 83 83 82 82 81 81 81 81 81   40
0480 81 81 81 81 81 81 82 82 83 83 84 85 86 87 88 89   37
0490 8A 8B 8D 8E 8F 91 93 94 96 98 9A 9B 9D 9F A2 A4   5C
04A0 A6 A8 AA AD AF B2 B4 B7 B9 BC BF C1 C4 C7 CA CD   88
04B0 CF D2 D5 D8 DB DE E1 E4 E7 EA EE F1 F4 F7 FA FD   5E
04C0 00 03 06 09 0C 0F 12 16 19 1C 1F 22 25 28 2B 2E   71
04D0 31 33 36 39 3C 3F 41 44 47 49 4C 4E 51 53 56 58   4F
04E0 5A 5C 5E 61 63 65 66 68 6A 6C 6D 6F 71 72 73 75   88
04F0 76 77 78 79 7A 7B 7C 7D 7D 7E 7E 7F 7F 7F 7F 7F   C0
```


0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 3
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
2 2 2 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 4 4 4
0 1 3 4 6 7 9 A C D F 0 2 3 5 6 8 9 0 1 2 4 5 7 8 A B D E F
0 A 2 B 3 C 4 B 3 B 3 B 3 C 4 C 4 C 0 6 E 6 C 3 C 4 A 2 A F

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 3
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 ■

Figure 2: PAPERBYTE[tm] *bar code version of listing 2. For details on how to read bar codes, see* Bar Code Loader, *a PAPERBYTE*[tm] *book by Ken Budnick.*

Approaching Game Program Design

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Chapel Hill NC 27514

One of the common applications of a personal computer system is developing and playing game programs. There are various ways the computer can be used in game playing. First, it can be used in the analysis of games such as poker and blackjack. The analysis has generally been done in an effort to get a deeper understanding of tactics and strategy. Another use is having the computer assist in the play of a game. Sports gives examples of this. The computer can analyze play patterns to provide the coach with information. In assisting, the computer can remember previous plays and provide advice on what moves should be made based on past experiences. Table 1 summarizes some of the ways computers can enter the field of gamesmanship.

The common use of the personal computer in games is as a game master. The program serves as a bookkeeper and a rule user. It enforces the rules, and, hopefully, explains them. A further use of a game program is where the program is a participant.

Most game programs act as game master and quite a few provide a game player function. Some games provide a form of advisor, but generally the advisor function is in the form of unrequested information warning the player when certain conditions have occurred.

Design

It may be obvious that the program design is a separate activity from coding the program. Rarely does it make sense to start programming right off. Quite often, someone starts programming because they understand part of the problem and believe it is easier to program the section that is known and let the rest fall into place. The problem with this method is that it is like building a house without a plan. It is much easier to do the plumbing and wiring as the rest of the house is being built. Likewise, the failure to have a plan of the program before coding begins can cause major changes in parts that were coded before the program design is complete.

For very simple game programs it is possible to go from concept to program with no intermediate steps. As the game program gets larger it gets increasingly difficult to avoid an intermediate step or steps. Doing a large game in a single leap from concept to program usually results in a rough program requiring extensive debugging and modification before it is functional. As changes occur, the program grows in complexity. Hopefully, the program converges on the desired result. Most often, the process and the end result leave something to be desired. If the program is to be used by anybody else, and especially if it may be modified by someone besides the designer, a thorough groundwork should be laid. First the game is designed, then comes the program design stage, followed by the implementation of the program.

Assuming that you already have a game design mapped out, we can discuss the actual design of the program. This discussion is for single terminal games and does not specifically cover either multiple terminal game program design or real time game program design. Program design is broken into two sections, external design and internal design. External design covers what the user of a game program sees and notices. Internal design discusses the implementation of the game.

External Design

The first suggested step is to write an abbreviated game description, such as listing 2, to show what you are trying to do. Try to answer some of the following questions. Who will be the end users of the game?

Game Master	Bookkeeper Rule User Rule Enforcer Rule Explainer
Game Player	Acts as one or more players.
Game Advisor	Provides analysis and suggests moves.

Table 1: There are three basic functions a computer may perform in game playing. It can keep track of the rules and permissible moves of an entire game; it may review the current state of the game and provide advice as to the best move; or it may act as an actual player. The game player function is actually composed of both the game master and advisor functions. The game master function notifies the game player function about the rules. The advisor function is used to decide which move will be made.

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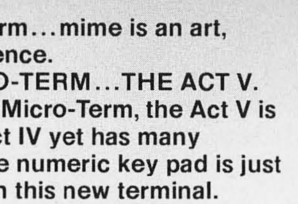
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Circle 219 on inquiry card.

```
Request for Input:
    HOUR 7, AT WHAT ANGLE DO YOU WISH TO SEND
    YOUR PROTON BOMB? 200
    HOW FAR OUT DO YOU WISH TO DETONATE IT? 150
Original Response:
    YOUR PROTON BOMB EXPLODED 14159.9 FROM THE
    ROMULAN SHIP.
New Response:
    AT ANGLE 200, RANGE 15,000
       EXPLODED 14159.9 FROM THE ROMULAN SHIP.
Original Ending:
    If successful:
       YOU HAVE SUCCESSFULLY COMPLETED YOUR MISSION.
    If unsuccessful:
       YOU HAVE ALLOWED THE ROMULANS TO ESCAPE.
New Ending:
    If successful:
       SHIP EXPLOSION AT ANGLE 217 DISTANCE 26100.
       YOU HAVE SUCCESSFULLY COMPLETED YOUR MISSION.
    If unsuccessful:
       A SHIP WENT INTO WARP DRIVE AT ANGLE 37 DISTANCE 10800.
       THE ROMULANS HAVE ESCAPED.
```

Listing 1: Feedback is an important part of a game program. Without information returning to the players it can be difficult to improve play strategy. The original program responses in the example were scanty and did not give much information about what was happening. In the original program the ending summary leaves the players wondering how to improve their games since it is impossible to tell exactly how close they were to winning. In the new version, it is possible to check over the response and alter strategy on the basis of the given information.

What age bracket will the end users be in? Is the same game playable by 5 year olds and by persons with doctorates? What is the target market? Will it be just a program or will it be a program product with the generalization, testing, and documentation that such entails? How long should the game run? What are the variations in the playing time? How does the game begin? A lot of game programs just begin. They give no prologue, no query to ask the user if the game is familiar and if the play procedure is understood.

In group simulation games, a person acts as moderator. The moderator normally gives an introduction, which provides orientation and instructions. When the simulation ends, the moderator provides a summary. This wrap-up allows the participants to discuss with the moderator what happened during the game.

Likewise, a game program should give the player feedback at the end. Every pinball machine and gaming device in an amusement park counts points on some basis to give the player a measure of performance; a game program should do likewise. In *101 Computer Games* the program for Orbit allows seven hours to shoot down a Romulan ship. If the seven hours pass, that is that. The player has no idea where the Romulan ship was when it left orbit. Similarly, even if the ship gets shot down by a photon bomb, the only result is that the player knows the ship has been destroyed. The simple addition of information such as the orbit and specific position in the orbit gives desirable feedback. Listing 1 shows this type of feedback in an example output. The player now knows whether or not the hypothesis being used was even close. Giving a recapitulation in a game program can keep the user coming back to play it again.

The amount of feedback given may depend on the output device. A teletypewriter is slow; a player may get impatient waiting for long messages to be delivered. A video terminal can display a screen full of information in very little time. Too much feedback may not be good, but a player does not have to read all the information presented. However, a player cannot use what a program does not give as feedback.

One area often overlooked when designing a program is causes of termination. In group simulation games, a moderator can be told to quit while ahead. A moderator can also determine if further playing is futile and can end the simulation. Some game programs are open ended and will run forever. A program should allow the user to terminate the program in an orderly fashion. Even better is the ability of the player to restart the game where it was stopped.

A part of the external design is what the user sees and does to begin and end a game. Another part of the external design is to determine how information is entered for play of the game.

Now that you have written down the goals of the game and some of the factors of the program, you should make some fake output. Show what a typical run of the game program might look like. Make up output showing how the program begins, how the play begins, and what introductory and help information is displayed. If turns are repetitive, only a few turns need be shown. Show what happens when the game ends.

The next step is for the program designer to make up a set of user instructions. The information shown in the sample output of listing 2 serves this purpose for a game called "Mazewizard." In some cases other

Listing 2: Game design outlines such as this are a great aid when developing a game. This type of written description helps to formulate clearly the main purposes of the game.

```
Game: Mazewizard Version 0
Description: Mazewizard is a game in which the player is a wizard in a three-dimensional
      maze attempting to collect treasure.
Playing Data:
      Age Level: Ten years to adult.
      Number of Players: One.
      Playing time:Ten to twenty minutes.
Game Start: Ask if the player wants a description of the game. If so, print out a brief
      description of the game and how moves are made.
Game Play: The player enters a move direction. Treasure is automatically accumulated.
      The portion of the maze that can be seen is printed.
Game Termination: Play ends three ways. First, half of the treasure is found. Second,
      the player encounters a fatal maze hazard, ending play. Last, a player requests
      termination by entering a move of no change. In all three cases, the total treasure
      found will be printed, and the average treasure found per move is printed.
```

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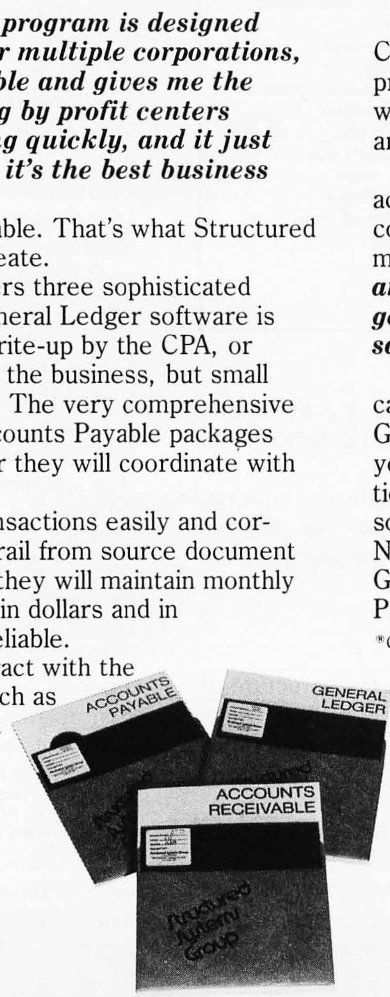
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Listing 3: This logic structure for a 1 player game indicates play cannot be stopped until the end of the game is reached. This is not always desirable; thought should be given to ending the game in some fashion such that it may be continued later from where it was stopped.

```
BEGIN       introduction
            (instruction if requested)
            initialization
PLAYGAME    loop till game over
                set up turn
                obtain player's move
                validate move
                echo move
                apply move
            end loop
END         summary
            stop
```

Listing 4: This logic flow is designed for a multiple user game. All of the players' moves are gathered before any processing is done. After all moves are made, the information resulting from the move processing is provided to all of the players.

```
BEGIN       introduction
            (instructions if requested)
            initialization
PLAYGAME    loop till game over
                set up turn
                loop till have all moves
                    set up move
                    obtain player's move
                    validate move
                    echo move
                end get move loop
                apply move
            end turn loop
END         summary
            stop
```

Listing 5: Another form of the multiple user game allows single move acquisition and processing. This type of approach would be useful in board games such as Monopoly where only one person moves at a time, yet the information from that move is needed by the other players before they can move intelligently.

```
BEGIN       introduction
            (instructions if requested)
            initialization
PLAYGAME    loop till game over
                set up turn
                loop till have all moves
                    set up move
                    obtain player's move
                    validate move
                    echo move
                    apply move
                end get move loop
            end turn loop
END         summary
            stop
```

information may be desired. It may be useful to list some features not implemented in this version.

At this point you have gathered information on what the program will look like to a user. Now let us see what the design of the actual program entails.

Internal Design

When designing the internal structure of the program, there are several areas which must be covered. These can be broken down into logic flow, algorithms, and data structure.

Some game programs have a structure similar to listing 3. This structure is for a one player game. It does not show a method of stopping the game before the conditions for the end of the game are met.

Multi-player games are somewhat more involved. The program may gather information from all players for a turn, then process that turn. This is commonly done in many business games. After all players make a move, the program processes the information, determines results and provides it to the players. An alternative approach is where the information is used after a player makes a move and before the next player enters a move. In programs of board and card games this is quite common. Listings 4 and 5 illustrate these two approaches.

The preceding discussion has covered the general logic flow of a program. The expansion of the basic steps is dependent on the game. The program designer needs to develop algorithms to implement the game. The major work will probably be in the move application portion of the program. The algorithms will manipulate various entities. These should be documented and named before coding begins. The larger the program, the more important is the documentation of the variables used in the program. Actions manipulate the variables. By analogy, the variables are the nouns and the actions are the verbs in the program, which is the instructions. For example, if a program deals with ships, the basic items may be ships, cargo, ports and oceans. The actions may include docking at port, setting sail, loading cargo, unloading cargo, setting course and speed, etc. The use of state diagrams can clarify the values that an item can have and how these values are allowed to change states. Gaps in game design are shown sometimes when state diagrams are used. Figure 1 shows a pair of state diagrams for the above shipping example. In figure 1 a ship is either in port or sailing. A ship can load or unload cargo only at a port. The two simple diagrams in figure 1 do not represent the state of the cargo when the ship is sailing. Figure 2 shows both the state of the ship and the state of the cargo at all times.

State diagrams suggest a method of segmentation or modularization; each routine could handle a single state transition. First the routine verifies that it is in the proper state(s) for the requested transition. Then it performs the variable manipulations that are part of the state change. The verification portion could be a separate routine that is part of the move validation section of the program. Alternatively, a state table could be used. The state table consists of new states indexed by the current state and the requested action. To make a move, find the current state in the table, index to the action being requested, and go to the new state indicated by that location. For some game

designs, state diagram usage will make little sense. Other games will lend themselves to state analysis very well.

Conclusion

In this article, I have covered an approach to the design of computer games. Planning the internals and externals of a game program can ease the actual programming and result in a game program that is more satisfying to the user. The discipline involved can and should make the inspiration and creativeness of a new game easier to realize.

The references in the bibliography are suggested to those involved in the design of game programs. The volume edited by Robert Horn is probably the best reference for game ideas.■

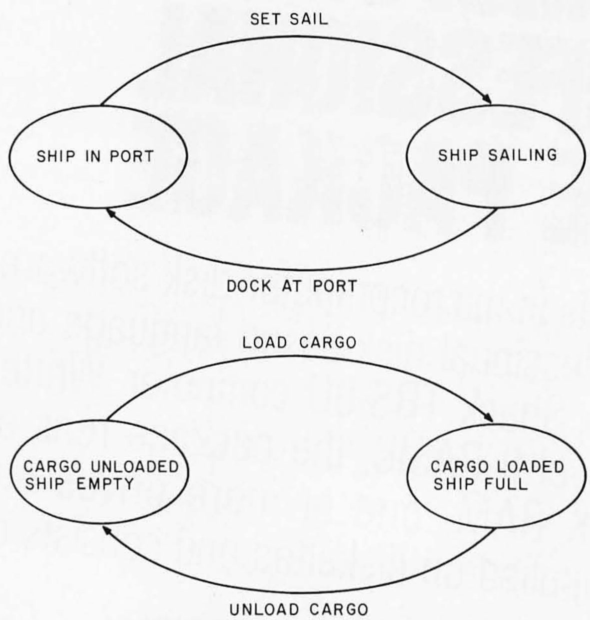


Figure 1: This pair of state diagrams can be used in the shipping example in the text. The first state diagram shows the pattern that is followed by the sailing and docking of a ship and its related states. The second diagram shows the states of the cargo that is on board the ship.

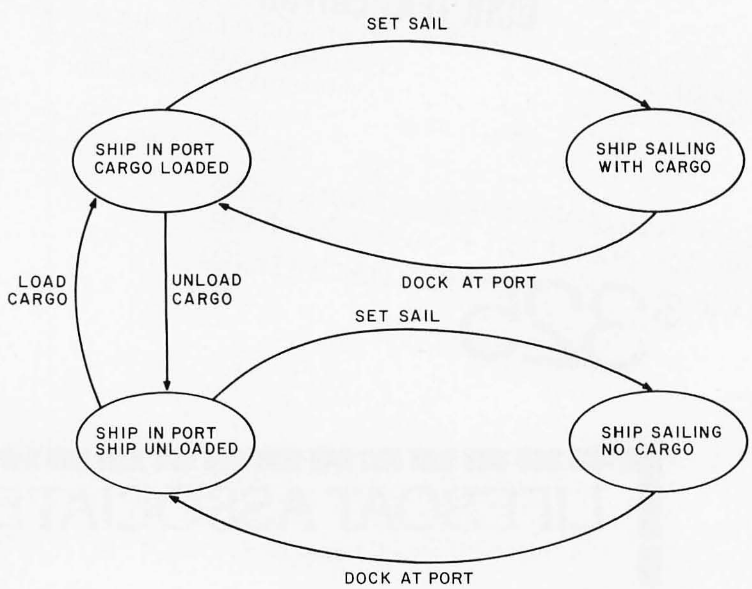


Figure 2: From the diagrams of figure 1 it is not possible to keep track of what the cargo is doing in relation to the state of the ship. For instance, can the cargo be unloaded when the ship is sailing? This diagram relates the state of the cargo with the state of the ship at all times.

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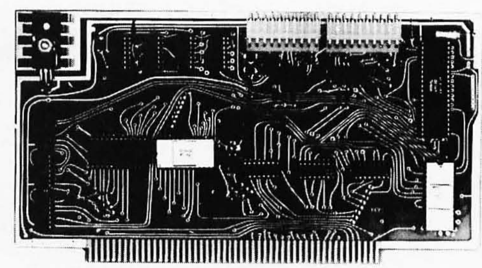
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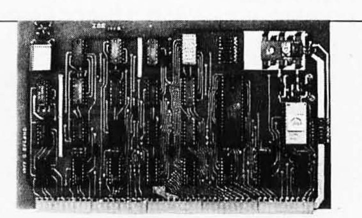
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Nybbles

Computerized Wine Cellar

Listing 1: Typical output from the Wine Cellar program showing how the system can search through data records.

```
                         WINE CELLAR

DO YOU WANT TO:

     1) ADD A NEW LISTING
     2) ACCESS EXISTING LISTINGS
     3) DELETE A LISTING
     4) GET NUMBER OF BOTTLES STORED
     5) CHANGE OUTPUT DEVICE
     6) END

?2

FILE ACCESS—

DO YOU WANT YOUR ACCESS RESULTS OUTPUT TO:

     CRT  OR  PRINTER?  PRINTER

FILE ACCESS—
HOW DO YOU WANT TO ACCESS?  BY:

     1) BOTTLE NUMBER
     2) TYPE (RED, WHITE, SPECIAL)
     3) VARIETAL NAME
     4) VINTNER OR PRODUCER
     5) SPECIAL NAME
     6) VINTAGE DATE
     7) PRINT ALL ENTRIES
     8) MULTIPLE SEARCH
     9) RETURN TO COMMAND LEVEL

?1

BOTTLE #? 165

BOTTLE # 165

CABERNET SAUVIGNON, CHARLES KRUG, 1973.
10TH. Large bottle in long term storage (#18). Soft, fruity wine, characteristic of
Krug tradition. Finigan 4/77, pg. 61. $2.69

(TYPE ↑ TO RETURN TO ACCESS LEVEL)
↑

FILE ACCESS—
HOW DO YOU WANT TO ACCESS?  BY:

     1) BOTTLE NUMBER
     2) TYPE (RED, WHITE, SPECIAL)
     3) VARIETAL NAME
     4) VINTNER OR PRODUCER
     5) SPECIAL NAME
     6) VINTAGE DATE
     7) PRINT ALL ENTRIES
     8) MULTIPLE SEARCH
     9) RETURN TO COMMAND LEVEL

?8

MULTIPLE SEARCH MODE—

HOW DO YOU WANT TO ACCESS?  BY:

     1) VARIETAL NAME + VINTNER
```

Rodney W Jolliffe
POB 2109
Alameda CA 94501

The blending of two hobbies can make each more interesting, and one can often enhance the satisfaction of the other. This has happened with me in the happy combination of computers and wines. My wife and I greatly enjoy the collecting and drinking of fine wines, and I also enjoy working with personal computers at home and work. Our wine cellar has grown to the point where, when we want to drink a particular wine, we hardly know what we have in our stock. While thinking about this dilemma I realized that perhaps I could put my Processor Technology SOL to work on the problem. I developed a program that stores information for each bottle in a BASIC file on a North Star disk for access at a later time.

The program has been immensely useful and has made finding a bottle for drinking much simpler. It has helped us to take our inventory; now it is much easier to know what we have in certain categories of wine (ie: Zinfandels from a specific winery); therefore we can purchase more wisely.

Usage Instructions

The storage file called CELLAR is set up for the storage of up to 260 bottles. As bottles are entered using the ENTER command, they are assigned a sequential bottle number beginning with bottle number one. When a bottle has been used, it may be deleted from the file with the DELETE command. When the next bottle is entered, it will be assigned the number of the first available space—either a deleted space where it will be assigned that bottle number or the first space at the end of the file where it will be assigned a new number. As each bottle is assigned a number, take some small adhesive circles (available in any stationery store) put the bottle number just

Listing 1, continued:

```
    2) VARIETAL NAME + DATE
    3) VINTNER + DATE
    4) RETURN TO ACCESS LEVEL

?1

VARIETAL NAME:  RHEIN

VINTNER OR PRODUCER: RAUNTHALER

RHEIN
RAUNTHALER

BOTTLE # 66

RHEIN, RAUNTHALER ROTHENBERG, 1976.
RIESLING SPATLESE, von Simmern. Nicely balanced, handsome wine. Finigan 5/77,
pg. 69.  $11.50

BOTTLE # 68

RHEIN, RAUNTHALER BAIKEN, 1976.
RIESLING SPATLESE. See bottle #67 for details. Keep to 1982+.  Purchased Jackson's.
$9.75

      SEARCH COMPLETED
(TYPE ↑ TO RETURN TO ACCESS LEVEL)
↑

FILE ACCESS—
HOW DO YOU WANT TO ACCESS?  BY:

    1) BOTTLE NUMBER
    2) TYPE (RED, WHITE, SPECIAL)
    3) VARIETAL NAME
    4) VINTNER OR PRODUCER
    5) SPECIAL NAME
    6) VINTAGE DATE
    7) PRINT ALL ENTRIES
    8) MULTIPLE SEARCH
    9) RETURN TO COMMAND LEVEL

?9

                    WINE CELLAR

DO YOU WANT TO:

    1) ADD A NEW LISTING
    2) ACCESS EXISTING LISTINGS
    3) DELETE A LISTING
    4) GET NUMBER OF BOTTLES STORED
    5) CHANGE OUTPUT DEVICE
    6) END

?6

                    CHEERS
```

assigned onto the label and attach the label to the cork end of the bottle for quick identification purposes.

Information stored in the file can be retrieved with several commands:

BOTTLE NUMBER:
Will print out the complete listing for that bottle.

TYPE OF WINE:
Will print out all entries of that type (red, white, special).

VARIETAL NAME:
Will print out all wines of that varietal name (ie: all Cabernet Sauvignon).

VINTNER NAME:
Prints out all wines produced by that vintner (ie: all Robert Mondavi).

VINTAGE DATE:
Prints out all wines that have entries for that year.

MULTIPLE:
Searches for three types of multiple entries; VARIETAL NAME and VINTNER NAME, VARIETAL NAME and VINTAGE DATE, VINTNER NAME and VINTAGE DATE. All of these search the file for any entry that has both characteristics and prints it.

ALL ENTRIES:
Prints out a listing of all current entries in the file.

A typical user session with the Wine Cellar program is shown in listing 1. The program always checks any of the operations performed with the user before actually executing them. This helps reduce the number of erroneous changes made to the file.

The complete Wine Cellar program listing with documentation and hints on using other disk systems and BASICs besides North Star BASIC is available from BYTE for \$1.50 postage paid. Please use the coupon below and order BYTE document #103.■

---

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Responses to the Queens

We received so many responses and letters to Terry Smith's article "Solving the Eight Queens Problem" (October 1978 BYTE, page 122) that we decided to have a one-time, special column.

*Following are several solutions and comments on the eight Queens problem. They range from adding graphics to the output to shortening the search time. All of these programs, except the Pascal versions, were run on our Apple and TRS-80 office computers. Several of the programs gave output so quickly that we barely had time to note the solutions. We thank all those who spent time on these programs for their comments. . . .*RGAC

8 Forum

Patching the Eight Queens

Paul J Kosicki
POB 18374
Denver CO 80218

I enjoyed Mr Smith's article on the eight Queens problem. I found it amusing that the problem solved by Mr Smith's program, described as ". . . a blow to structured programming. . .", is the same problem used by Dr Dijkstra in his classic illustration of the development of a structured program (see *Structured Programming,* Dahl et al, Academic Press, New York, 1972, pages 72 thru 82).

Both programs overlook an observation which would reduce the total solution time by one half. This is that the reflection of any solution about the axis between the fourth and fifth ranks of the board is also a solution. As the Queen on file (1) starts on rank (1) and moves to higher ranks only after all possible solutions with the Queen on that rank are generated, all reflected solutions with Queen(1) on rank(1) gives all solutions with Queen(1) on rank(8). Therefore, by moving Queen(1) only to rank(4) and reflecting all of these solutions, we generate all solutions in half the time.

In Mr Smith's program, the following changes will accomplish this:

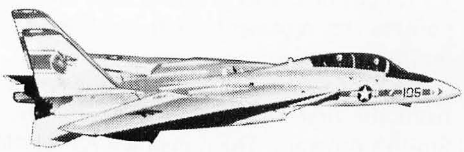
```
362 IF C # 1 THEN 380
364 IF E = 4 THEN 480.
```

Lines 250 thru 321 are copied in line, with the first line of the second copy changed to:

```
322 FOR X = 1 TO 8.
```

This will print the reflected solutions as they occur.■

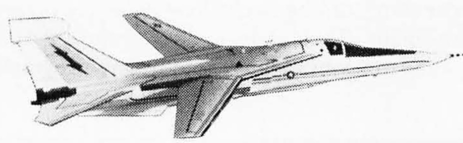
Circle 137 on inquiry card.



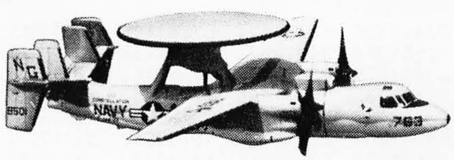
F 14 A TOMCAT



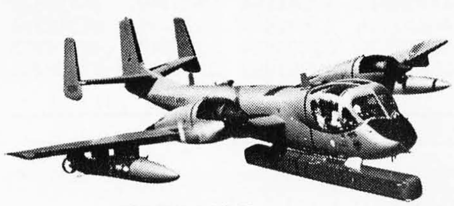
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8 Forum

23 or 12 Solutions?

James C Puckett
2201 Eastlawn Dr Apt 12
Midland MI 48640

I was intrigued by Terry Smith's clever solution to the eight Queens problem. His statement, "There are 92 solutions of which 23 are discrete," aroused my curiosity.

It seemed logical to me that any unique solution to the problem should have eight variations: the solution, its mirror image, and each of these viewed from each of the four sides of the board. Therefore, to test the solutions from Mr Smith's program, I wrote a program to generate the eight variations for each solution from the program and to test the following solutions for repetitions. This program used the 8 digit number to represent each solution as Mr Smith suggested.

This program found 12 unique solutions from the first 18 solutions generated by Mr Smith's program. The remaining 80 solutions from his program turned out to be variations of these 12. Thus it would seem that there are 96 solutions, 12 of which are unique.

I made no effort to determine if there might be other unique solutions, but perhaps a mathematician among the readers has already derived an equation to determine the maximum number.

This exercise points out the necessity of checking data generated by programs before relying on it too heavily. Sometimes this checking can be as challenging as the original problem. Table 1 is a copy of the solutions and variations as generated by my program.■

Table 1.

	UNIQUE	MIRROR	UNI+90°	MIR+90°	UNI+180°	MIR+180°	UNI+270°	UNI+270°
1	36428571	17582463	15863724	84136275	82417536	63571428	57263148	42736851
2	35286471	17468253	16837425	83162574	82531746	64713528	47526138	52473861
3	47382516	61528374	24683175	75316824	38471625	52617483	42861357	57138642
4	63728514	41582736	25713864	74286135	58417263	36271485	53168247	46831752
5	63724815	51842736	25741863	74258136	48157263	36275184	63185247	36814752
6	64285713	31758246	26174835	73825164	68241753	35714286	46152837	53847162
7	37286415	51468273	26831475	73168524	48531726	62713584	42586137	57413862
8	52468317	71386425	27368514	72631485	28613574	47531682	58413627	41586372
9	42736815	51863724	27581463	72418536	48136275	57263184	63581427	36418572
10	46827135	53172864	35281746	64718253	46827135	53172864	35281746	64718253
11	36824175	57142863	35841726	64158273	42857136	63175824	37285146	62714853
12	57248136	63184275	36258174	63741825	36815724	42751863	52814736	47185263

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An Apple and the Queens

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Chemistry Dept
Harvard University
Cambridge MA 02138

Terry Smith's excellent article concerning the eight Queens problem prompted me to write my own eight Queens program for the Apple II. Broadly speaking, the logic is a synthesis of Smith's second and third methods, with a few judicious improvements. There are several advantages to this program vis-a-vis the published one as follows:

1. It is far shorter, and uses considerably less memory.
2. It is much faster, taking approximately *5 seconds* per solution.
3. Apple's color graphics allows the user to watch as the computer "searches" for a solution.

My program is shown in listing 1. It is written in integer BASIC and is easily translated to other systems. The disadvantage of this program, in its present form, is that it does not allow one to systematically search for *all* the solutions.■

Listing 1.

```
)LIST

  10 CALL -936: GR : DIM A$(5),Q(
     8)
  20 COLOR=14: FOR I=2 TO 32: HLIN
     2,32 AT I: NEXT I
  30 COLOR=2: FOR I=1 TO 33 STEP
     4
  40 HLIN 1,33 AT I:VLIN 1,33 AT
     I: NEXT I: GOTO 100
  50 COLOR=14: FOR I=1 TO C-1: PLOT
     (I*4)-1, (Q(I)*4)-1: NEXT I
 100 FOR C=1 TO 8:X= RND (8)+1
 110 CTR=1: IF C=1 THEN 180
 120 FOR I=1 TO C-1
 130 IF Q(I)<>X AND ABS (Q(I)-X)
     <>ABS (I-C) THEN 170
 140 X=X+1: IF X=9 THEN X=1
 150 CTR=CTR+1: IF CTR=9 THEN 50
 160 GOTO 120
 170 NEXT I
 180 Q(C)=X: COLOR=9: PLOT (C*4)
     -1, (Q(C)*4)-1
 190 NEXT C
 200 VTAB 23: PRINT "HERE IS ONE SOLU
     TION.": PRINT
 210 INPUT "DO YOU WANT ANOTHER? (Y O
     R N)",A$
 220 PRINT : IF A$="Y" THEN 50
 230 END
```

8 Forum

Checking Permutation Generation

```
100 REM 8 QUEENS
110 DIM X(7,7), I(7)
120 INPUT N \ M = 1 \ X(0,0) = 0
130 I(M) = 0
140 FOR J = 0 TO I(M) - 1 \ X(J,M) = X(J,M-1) \ NEXT J
150 X(I(M),M) = M
160 FOR J = I(M) + 1 TO M \ X(J,M) = X(J-1,M-1) \ NEXT J
170 IF M = N THEN 180 \ M = M + 1 \ GO TO 130
180 FOR J = 0 TO N - 1 \ FOR K = J + 1 TO N
190 IF ABS(X(K,N) - X(J,N)) = K - J THEN 220
200 NEXT K \ NEXT J
210 FOR J = 0 TO N \ PRINT X(J,N); \ NEXT J \ PRINT
220 IF I(M) = M THEN 230 \ I(M) = I(M) + 1 \ GO TO 140
230 IF M = 1 THEN 120 \ M = M - 1 \ GO TO 220
240 END
```

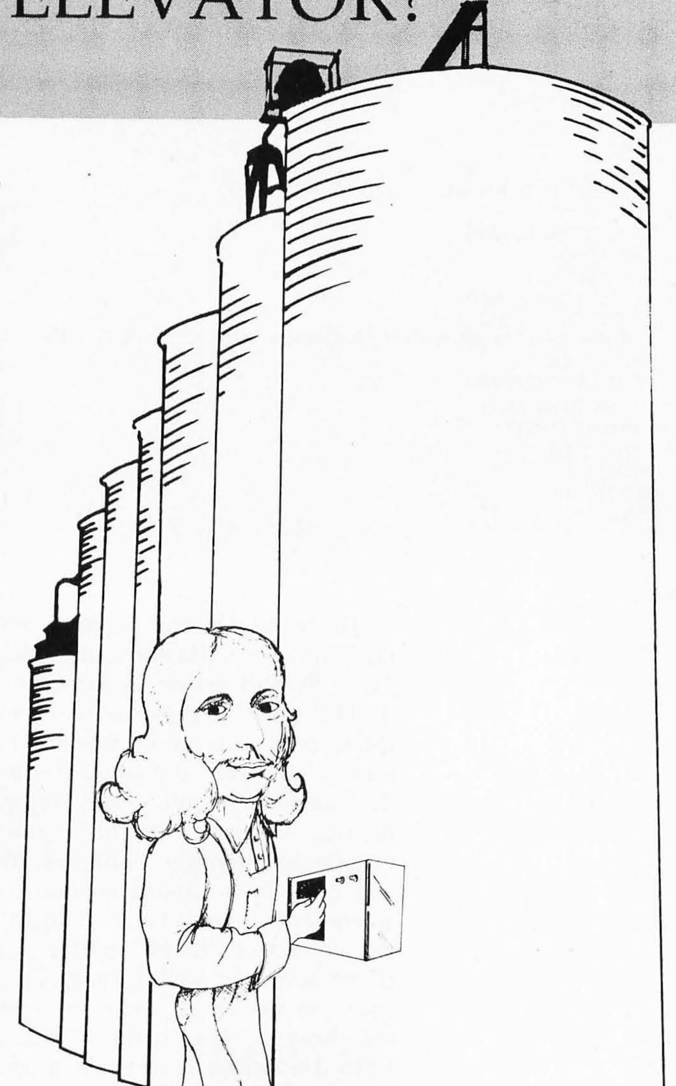
Listing 2.

James C Wilcox
2200 Via Alamitos
Palos Verdes Estates CA 90274

I found "Solving the Eight Queens Problem," by Terry Smith, to be an entertaining description of an example of the actual problem solving process. However he asked the wrong "friends" about generating the 8! permutations of the numbers 1 to 8, which actually is not a "difficult task" at all. In fact the algorithm seems to be rather well-known; however, I can't recall where I first heard of it. Without implying that a solution based upon generating these permutations would be better than the solution presented, I would like to describe the method of generating permutations which may be of general interest for other applications as well.

Let us use 0 thru 7 instead of 1 thru 8. We start with the permutations of 0, that is: 0. We take 1 and place it before and after each digit of each permutation of 0 to get the permutations of 0 and 1, that is: 10, 01. We take 2 and place it before and after each digit of each permutation of 0 and 1 to get the permutations of 0, 1, and 2, that is: 210, 120, 102, 201, 021, 012. We continue in this pattern with 3, 4, 5, 6, and 7. We arrange the code so that we generate each permutation of 1, 2, 3, 4, 5, 6, 7, and 8 digits only once—and we test each permutation for the presence of Queens on the same diagonal (absolute value of slope of line connecting Queens equal to 1) immediately after generating it so that we don't have to "file all those 40,320 8 digit numbers." The BASIC program in listing 2 solves the problem for boards up to 8 by 8 (N = 7). It took 5050 seconds to find all 92 solutions to the 8 by 8 problem on my H11. Generating the permutations required 2495 seconds or 62 ms per permutation. Testing the permutations required 2555 seconds or an average of 63 ms per test. The time required for each test varies widely, with a successful permutation taking the longest. Lines 180 thru 210 are peculiar to the eight Queens problem and can be replaced by code appropriate to other problems involving permutations. The rest of the code generates the permutations.■

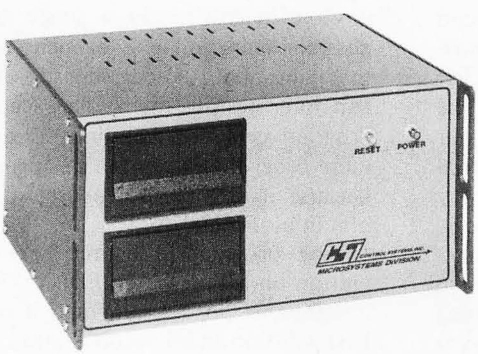
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Systematic Approach to the Eight Queens

```
  10  DIM R(8)
 100  C=0
 200  C=C+1
 300  R(C)=0
 400  IF R(C)<8 THEN 600
 500  C=C-1
 510  IF C=0 THEN 9999
 520  GOTO 400
 600  R(C)=R(C)+1
 605  IF C<2 THEN 660
 610    FOR C1=1 TO C-1
 620    IF R(C)=R(C1) OR R(C)+C=R(C1)+C1 OR R(C)-C=R(C1)-C1 THEN 400
 650    NEXT C1
 660  IF C<8 THEN 200
 700    FOR C1=1 TO 8
 710    PRINT R(C1);" ";
 720    NEXT C1
 730  PRINT
 740  GOTO 500
9999  END
```

Listing 3.

The eight Queens problem is indeed a fascinating one. However, the discussion in Terry Smith's article in the October 1978 BYTE, while it presents some very good ideas, cries out for comment. The fundamental algorithm presented has merit, yet the implementation leaves much to be desired. Given a specific algorithm, our experience strongly indicates that trial and error is an absurd method to employ whenever an organized thought process can be applied. As Mr Smith's search algorithm appeared well-defined, we chose to take the structured route to implementing the program. The results of this endeavor yielded a drastic decrease in program development time as well as enormous benefits in program space, data storage, and execution speed. Could it be an accident that code produced as such is so easily readable? A couple of hours well-invested in structured coding is an excellent trade for several days of cut-and-try frustration.

It seems unlikely that Terry has the most efficient program implementation for his algorithm. Why store the entire chessboard when all that is required is a row with eight column positions, or if you prefer, a column with eight row positions? Now all that we need to identify are the conditions required for avoiding positions of attack. Two Queens on a chessboard must not share a common row, a common column or a common diagonal in either direction. That constitutes four conditions.

We can assure different columns by making the column number the subscript of a one-dimensional row array. We can store the row number of each Queen in the column position of the row array. For example: if R(2)=5 there is a Queen in the fifth row of column 2. Now we simply assure that there are no duplicate values stored in the R array. For two Queens at points (X,Y) and (X',Y') one diagonal is shared if X−X'=Y−Y', while the other diagonal is shared if X+X'=Y+Y'. The last three of these conditions may be tested in a single BASIC statement (see line 620 of the accompanying program listing 3). It should be evident that the four conditions defined above did not come from a hit or miss process. It is clearly more efficient to use eight stored values than to use 64. Clearly it is more efficient to do a single test on all possible pairs in an 8 element array than to roam about a chessboard setting flags and later testing them. The accompanying program generates solutions in exactly the same order that Terry Smith's program does, because it uses the procedures suggested by him in his article.

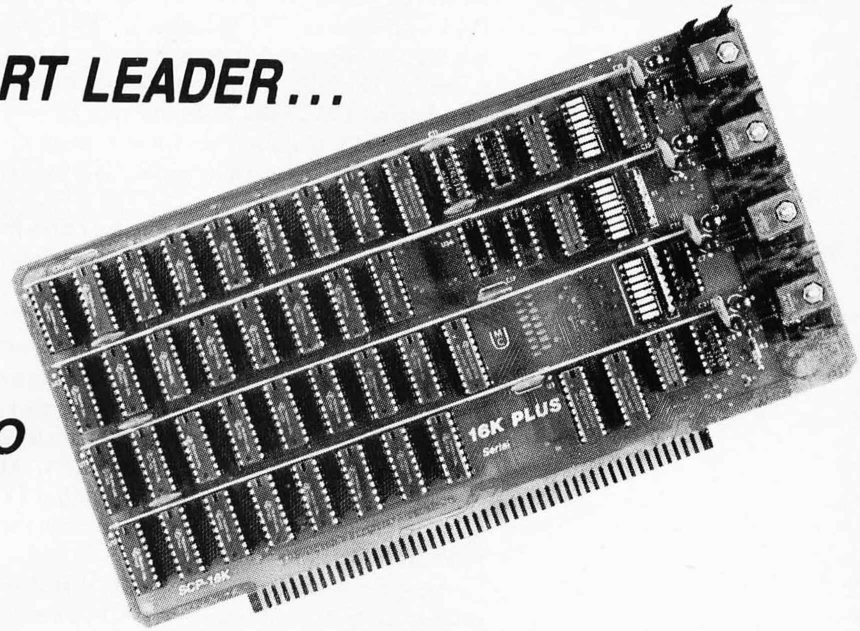
The program in listing 3 ran to completion on a timeshared PDP-11/70 in about 2 minutes. On a Cromemco it printed the first solution in 44 seconds and ran to completion in less than 14 minutes. Terry Smith's program, when run on the Cromemco, printed the first solution in 3 minutes and 18 seconds and printed the 92nd solution in 1 hour and 9 minutes. But the best time was logged by coding our solution in FORTRAN. That ran to completion on the Cromemco in less than 30 seconds. Imagine what an IBM 370 would do.

Possibly Terry Smith's greatest oversight in his search for an efficient program to implement his excellent algorithm is that his program has no termination! When will people realize that efficient, elegant code is not complicated and filled with mystery and magic? Efficient, elegant code is simple, clear and often short.■

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8 Queens Forum

APL Permutations

William Rubenstein
500 Rebecca Dr
St Charles MO 63301

Terry Smith's article concerning the eight Queens problem was a disappointment. The problem has been treated instructively and solved elegantly by Wirth (in *Algorithms + Data Structures = Programs*), and the muddy, unorganized approach to a solution taken by Mr Smith demonstrates poor problem solving skills which should not be perpetuated. His inability to write a program which generates permutations is to be expected.

I am offering a permutation function in APL. Input to the function consists of two vectors, X and Y. X is the left side (or the high order end) of a partially completed permutation. Y is the set of available symbols to be concatenated with X. At statement 1, I (a local variable) is initialized to 1. If Y contains only one element, statement 2 will be executed next, else statement 4. At statement 2 the completed permutation (Y concatenated with X) is displayed and the function is exited at statement 3.

At statement 4 an element of Y is concatenated with X and becomes X to a recursive invocation of the function. The Y for the recursive invocation is all elements of the set Y with the exception of the one which was concatenated with X. Further recursive invocations will eventually reduce the set Y to one element and cause output of a completed permutation. Statement 5 steps the local variable I and causes a return to statement 4 until each element of Y has been processed.

In an initial invocation (see listing 4), X is an empty vector and Y contains all symbols of the set to be permuted. The method assures a systematic and complete production of all permutations. The Y vector may be either numeric or alphabetic.

My solution is a "first cut" at the problem. I am certain that much better solutions will occur to me and are known to others. A nonrecursive solution can be found in Dr Dijkstra's book *A Discipline of Programming.*

It could be that Smith's problem stems from his choice of the BASIC language, whose lack of recursiveness and local variables (among other deficiencies) presents constant barriers to problem solving. I recommend APL or Pascal to him. I also recommend that he find some different "software experts" with whom to consult.■

Listing 4.

```
      ∇PERM[⎕]∇
    ∇ X PERM Y;I
[1]   →L×ι(I←1)≠ρY
[2]   X,Y
[3]   →0
[4] L:(X,Y[I])PERM(I≠ιρY)/Y
[5]   →((ρY)≥I←I+1)/L
    ∇

   '' PERM 'ABCD'
ABCD
ABDC
ACBD
ACDB
ADBC
ADCB
BACD
BADC
BCAD
BCDA
BDAC
BDCA
CABD
CADB
CBAD
CBDA
CDAB
CDBA
DABC
DACB
DBAC
DBCA
DCAB
DCBA
```

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8 Forum

The Queens Encounter MUMPS

Frank Freeman
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Littleton CO 80123

I enjoyed reading the solution to the eight Queens problem by Terry Smith. The method is, indeed, very nonstructured. So, I hope not vindictively, I did it with a structured method. That is, I coded the solution in eight lines of MUMPS code (see listing 5); and ran it on my microNOVA. The computer printed the 92 solutions in 15 minutes 30 seconds.

Listing 5.

```
A      F  A=1:1:8 S Q(A)=0,H(A)=0 F B=1:1:8 S D(A-B)=0,E(A+B)=0
       S  A=1,B=0,Q(0)=0
R      D  T,U G:A R Q
T      S  B=B+1 Q:B >8  G:H(B)!D(A-B)!E(A+B)  T
       S  Q(A)=B,H(B)=1,D(A-B)=1,E(A+B)=1 Q
U      I  B<9 S A=A+1,B=0 Q:A <9  D  P
       S  A=A-1,B=Q(A),H(B)=0,D(A-B)=0,E(A+B)=0 Q
P      W  ! F J=1:1:8 W Q(J)
```

Here is the structure, as I verbalized it after writing the program:

A: initialize the test points. There are eight vertical columns; eight horizontal rows; and 30 diagonals, all set to "false."

R: main loop. Exit: no more solutions.

T: test a column for the next nonattacked point. Valid, set test points to "true." Invalid, top of row: B=9.

U: try another column. Valid test: next column: A=A+1. If A is greater than 8, print result, and "fall thru" to invalid test: back up a column and set its test points to "false."

P: print result.

Voila! A return blow from structured programming. My MUMPS which combines the interpreter, a data base handler, and an operating system cost $3000.■

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8 Forum

Eight Calculating Queens

Bill White
113 Wayside Ct
Cherry Hill NJ 08034

Terry Smith's article on the eight Queens problem brought back fond memories of the first time I "solved" the problem—more than 20 years ago, on an IBM 650. Just for the fun of it, I resurrected my program and adapted it to a programmable pocket calculator—the Texas Instruments SR-56. Listing 6, the resulting 100 step program, is shown. The running time for the entire set of 92 solutions is around 14 hours.

A word or two about the algorithm underlying this program—the problem becomes quite a bit simpler if it is restated from a geometric to a numeric orientation, namely:

> Determine all 8 digit numbers of the form
> $D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8$ —

consisting of all the digits 1 thru 8 such that the absolute value of the difference of any pair of digits D_a and D_b does *not* equal the difference between their relative positions in the number, ie:

$$|D_a - D_b| \neq |a - b|$$

As a matter of further interest, I programmed the same approach on my Signetics 2650 microprocessor. The program, with initialization but excluding display steps, required 63 bytes of memory, and it took a little less than 4 seconds to display all 92 solutions on my screen.

I feel that four further comments on Mr Smith's article are relevant.

1. The number of unique solutions to the Queens problem is 12, not 23 as reported. This becomes more obvious when the solutions are represented as numbers rather than as geometric figures as stated

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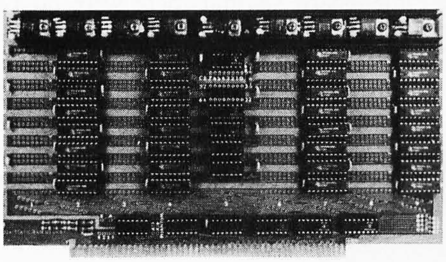
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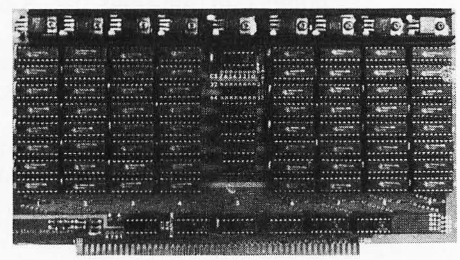
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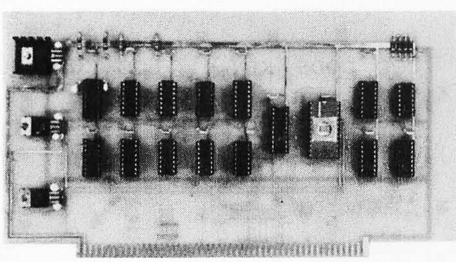
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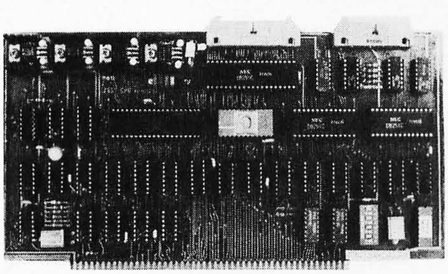
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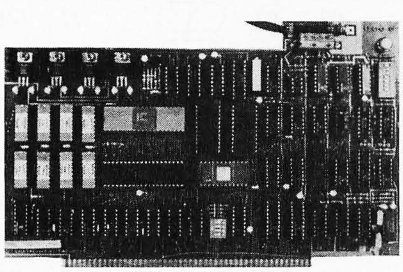
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before. With no convention defined for displaying a "solution," we are free to define the "home position" (1 in Di) as occupying any of the 4 corners of the chessboard. Also, we are further free to measure the digit values Di either horizontally or vertically from the home position, with the digit position i being measured in the other (vertical or horizontal) direction. Thus, each solution is one of a family of eight identical solutions (ie: the first solution, 15863724, leads immediately to the solutions 17582463, 36428571, 42736851, 57263148, 63571428, 82417536, and 84136275). The "sharp" reader will note that the total number of solutions, 92, is not divisible by 8. The reason is that one of the solutions—35281746 in its minimum form—is partially symmetrical and generates itself as a variation.

2. Mr Smith suggests that his next problem will be to substitute "Maharajahs" for Queens, where a Maharajah combines the moves of Queen and Knight. Inspection of the solutions will demonstrate that this is impossible—any solution of the Maharajahs problem must also be a solution to the Queens problem, and each of the solutions to the Queens problem has at least one pair of pieces that are a Knight's move apart.

3. A more interesting variation to the problem is to generalize the problem for an n by n chessboard.

4. In the 1950s, a game manufacturer had a somewhat popular game consisting of an 8 by 8 pegboard together with eight sets of colored pegs, each set a different color and consisting of eight pegs. The object of the game was to place all 64 pegs into the board so that there were no two pegs of the same color in any horizontal, vertical, or diagonal row. If you try to program this problem, you'll find it very difficult to debug. (A clue is that the game manufacturer offered a $1000 prize to anyone who could send in a solution—and he's still in business.)■

Listing 6.

LOC	CODE	KEY	LOC	CODE	KEY	LOC	CODE	KEY	LOC	CODE	KEY
00	38	*CMs	25	33	STO	50	94	=	75	34	RCL
01	00	0	26	03	3	51	37	*x=t	76	01	1
02	32	x≷t	27	34	RCL	52	06	6	77	64	x
03	34	RCL	28	01	1	53	03	3	78	01	1
04	00	0	29	33	STO	54	28	|x|	79	00	0
05	35	SUM	30	04	4	55	74	−	80	74	−
06	01	1	31	01	1	56	34	RCL	81	29	*INT
07	92	•	32	35	SUM	57	03	3	82	33	STO
08	01	1	33	03	3	58	94	=	83	00	0
09	30	*PROD	34	34	RCL	59	12	INV	84	94	=
10	01	1	35	04	4	60	37	*x=t	85	33	STO
11	34	RCL	36	37	*x=t	61	03	3	86	01	1
12	02	2	37	00	0	62	01	1	87	22	GTO
13	74	−	38	03	3	63	27	*DSZ	88	06	6
14	08	8	39	64	X	64	02	2	89	03	3
15	33	STO	40	01	1	65	04	4	90	01	1
16	00	0	41	00	0	66	01	1	91	35	SUM
17	94	=	42	74	−	67	12	INV	92	09	9
18	37	*x=t	43	12	INV	68	35	SUM	93	34	RCL
19	09	9	44	29	*INT	69	02	2	94	01	1
20	00	0	45	33	STO	70	34	RCL	95	41	R/S
21	01	1	46	04	4	71	02	2	96	22	GTO
22	35	SUM	47	74	−	72	37	*x=t	97	07	7
23	02	2	48	34	RCL	73	09	9	98	05	5
24	00	0	49	00	0	74	09	9	99	41	R/S

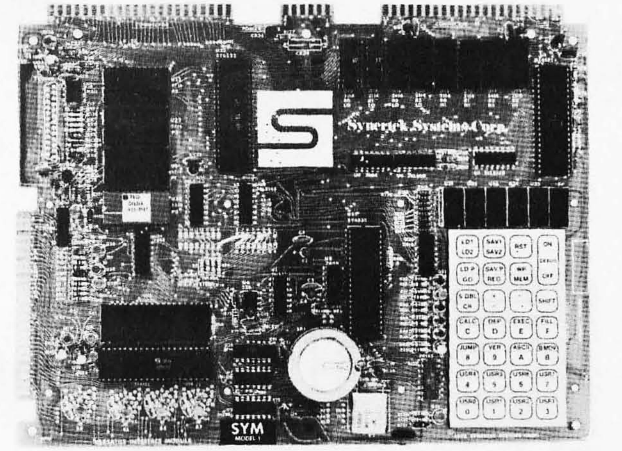
Registers

0	Trial Digit
1	Solution
2	Number of digits
3	△
4	Partial solution
5	8 ———
6	Number of solutions

Execution Notes: Load Program, (RST), (R/S), read solution. **Be Patient!!**

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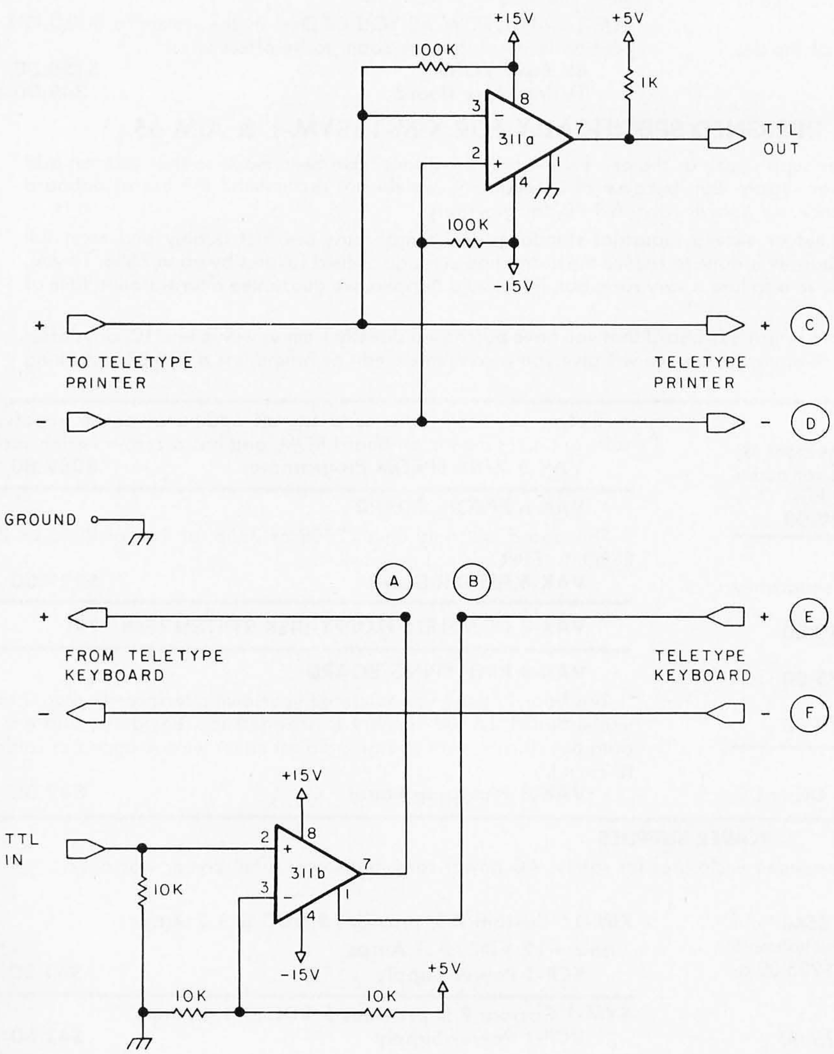


Figure 1: Interface circuit for connecting a TTL compatible circuit with RS-232.

In a small computer system with an ASR 33 Teletype-compatible terminal it would be convenient to connect a video terminal or a cassette interface to work in parallel with the terminal. Figure 1 shows a simple circuit with only two integrated circuits and six resistors which can convert a 20 mA current loop format to RS-232 format or to standard transistor-transistor logic (TTL) format. This circuit uses two 311 comparators, one in parallel with the wires to the printer and one in series with the wires from the keyboard. The 311 chips allow this circuit to be used with a microprocessor voltage range of ±15 V. Consequently, this circuit can be directly used with most types of 20 mA current loop interfaces.

The circuit shown is designed to interface with standard TTL levels. For example, this can be connected to a cassette interface board (S D Sales) to make your cassette look like a paper tape punch/reader. If you use it in this way, a switch can be installed, shorting A to B in order to eliminate the echo to the microprocessor during record. This switch is then opened during play. It is also possible to operate without a Teletype altogether by installing a switch which places a 15 ohm resistor across the printer wires (C and D) and shorting the keyboard wires (E and F).

In order to convert this circuit to RS-232, simply reconnect pin 1 on the 311 (A) from ground to −5 V. If your system uses ±12 V then put −12 V on pin 1 instead of −5 V and connect the pull up resistor (1 k located at pin 7) to +12 V instead of +5 V. If your microprocessor system only uses a positive supply to generate and receive the 20 mA current loop, then it is possible to save the negative power supply. Just use ground instead of the −15 V supply to pin 4 of both comparators.■

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CURSOR	Blinking block

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Model 501 — 115 volts, 60 Hz, 100 watts nominal
Model 502 — 230 volts, 50 Hz, 100 watts nominal

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Continued from page 10

have RATFOR for the PDP-11s in the Engineering Faculty and the main UNIVAC 1100/10, the latter which the author did. The penalty in machine code length works out to only 5% to 10% while compilation time is roughly twice (once through RATFOR and once through FORTRAN). This is offset by the need for less recompilation. In fact, getting a program to run first time is no longer a matter of luck.

I wholeheartedly support Pascal, but if your favorite computer (or local installation) does not have it yet, don't despair. As an interim solution, get a copy of *Software Tools* and write a RATFOR preprocessor. You may, as I did, learn a few things about language translation in the process.

I feel that users of RATFOR can make the transition to Pascal painlessly. Perhaps people could be weaned off FORTRAN in this way? Incidentally, the rest of *Software Tools* is very readable and gives good code for utilities such as an editor and a text formatter.

One small grouse: I feel that braces make better block markers than begin . . .end tokens as they clutter the page less.

Sue-Ken Yap
4 Pesiaran Syed Putra
Kuala Lumpur 08-06
MALAYSIA

USE OF DESCRIPTIVE VARIABLES

I would like to make one criticism about the Pascal program, Chess 0.5, by Peter Frey and Larry Atkin ("Creating a Chess Player, Part 2: Chess 0.5," November 1978 BYTE, page 162). Although their program was not written solely to demonstrate the merits of Pascal as a programming language, it remains an important showcase of the language. In addition, I feel that people unfamiliar with the language should realize how a minor change can improve the program and demonstrate more fully the power of the Pascal language.

The one change is to use long, descriptive procedure and variable names throughout the program thus following the spirit and letter of the Pascal language definition. By doing this, ZK becomes MAXSCHDEPTH and ZW becomes MOVESTKLIM. The increased readability is obvious. Readers who feel that the advantage gained by using longer names is not worth the increased coding and program entry effort will find that effort more than repaid when the program has to be corrected or extended sometime in the distant future, usually not by the original programmer.

Incidentally, I have just received confirmation that UCSD Pascal is now up and running on an Apple II.

Paul Kelley
The Analysts
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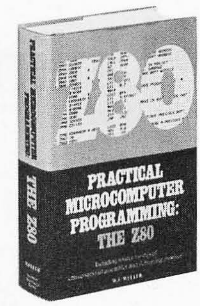
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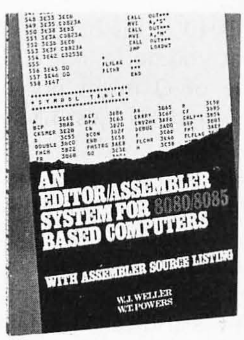
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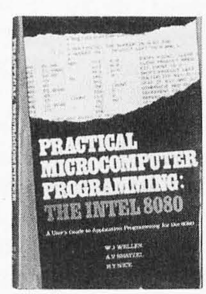
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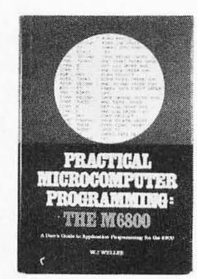
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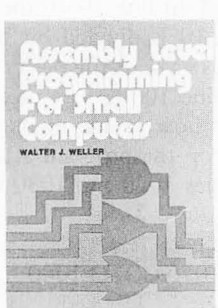
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The Apple II, which I own, is a fine computer, especially since most programs that interest me get along quite well with integer arithmetic. Text editing, graphics, and the music programs I experiment with have little need of decimal notation or quantities. Besides, if I really need numbers like 3.14159 I can always load Apple's Applesoft BASIC which has *floating point* arithmetic.

The problems involved in using integer arithmetic show up occasionally when I need to perform a division, though. If you add, subtract or multiply two integers, you get an integer. But if you divide one integer by another, you may or may not get an integer result. From a mathematical standpoint, integers are *closed* under addition, subtraction, and multiplication, but not under division.

I started to write a program to do real division on the Apple II. I thought it would be difficult, but it turned out to be very easy. Let us say you want to divide X by Y and print the answer to N decimal places. Listing 1 does the job, assuming X, Y and N are defined elsewhere.

Line 1020 determines the integer portion of the quotient. If X is 10 and Y is 3, Q is calculated to be exactly 3. This is, after all, integer division. Since we have the whole number part of the answer, line 1030 prints it. The semicolon means leave no space between the item just printed and the next item to be printed. The next item is a period (used as a decimal point). The final semicolon makes sure that the rest of the answer will be printed immediately after the decimal point.

```
1020   Q=X/Y
1030  PRINT Q;".";
1040   X=(X-Q*Y)*10
1050   Q=X/Y
1060  PRINT Q;
1070   N=N-1
1080  IF N>0 THEN GOTO 1040
1090  END
```

Listing 1: The BASIC program for unlimited integer division is really quite simple. It is explained fully in the text.

Line 1040 is the heart of the routine. It does what you do in long division. The original value of Q might not be exactly the right answer. Q is most likely too small (at best it is exactly right). By how much is it too small? You can find out by calculating the quantity QXY, and then subtracting that from X. In other words, check the division by multiplication (QXY) and see how much it missed X by subtraction. The quantity X−(QXY) is also called X MOD Y or, more simply, the remainder obtained after dividing X by Y. If your BASIC package has a modulus (MOD) function (as the Apple II BASIC does), you can simplify line 1040 to:

1040 X = 10(X MOD Y).

In long division, any remainder is handled by writing it down, and putting a 0 after it. Try performing a division and see. In the computer, multiplying by 10 puts a 0 after a number. Line 1040 imitates what you do by hand. Then, in line 1050, the remainder multiplied by 10 is divided by the original divisor, Y. This gives us the next digit, which is printed in line 1060. The next two lines merely count how many digits have been printed and stop the program after N digits. If you take lines 1070 and 1080 and replace them with:

1070 GOTO 1040

then you get truly unlimited precision. As long as you keep the computer running, it will turn out digits and they will all be correct. In the Apple II this means that no calculation ever exceeds 32,767. This is most likely to happen in line 1040. If you are using the modulus function, this can happen without getting a message and an incorrect result can appear. With the original line 1040, either the answer is exactly correct or the program halts.

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you will find that most decimal expansions of fractions repeat rather quickly. 1411 divided by 999 is 1.412412412 with the expression 412 repeating forever. More interesting is the quotient of 437 divided by 463, shown in table 1. *[Incidentally, 355 divided by 113 gives a good approximation of π. . . .*CM*]* While most decimal expansions repeat quickly, every decimal expansion of a fraction is a repeating decimal. It is not too hard to prove this, but the proof is a bit outside the realm of this article.

To make this into a demonstration, I use the program in listing 2. Lines:

```
1090 PRINT
1100 RETURN
```

are added to convert the routine into a subroutine, and the request for a new numerator appears on a new line, not just after the last quotient.

*[Once you've been using this routine for a while, try dividing some prime numbers. Of particular interest is the quotient of 99991 divided by 99989. So far we have generated 2500 decimal digits for this value at the BYTE offices without encountering a repetition. . . .*RGAC*]* ■

1	0	0	2	2	9	3	5	7	7	9	8	1	6	5	1	3	7	6	1	4	6	7	8
8	9	9	0	8	2	5	6	8	8	0	7	3	3	9	4	4	9	5	4	1	2	8	4
4	0	3	6	6	9	7	2	4	7	7	0	6	4	2	2	0	1	8	3	4	8	6	2
3	8	5	3	2	1	1	0	0	9	1	7	4	3	1	1	9	2	6	6	0	5	5	0
4	5	8	7	1	5	5	9	6	3	3	0	2	7	5	2	2	9					

Table 1: The result of dividing the number 437 by 436. The last three digits (229) begins the repetition sequence. Quite often, dividing two numbers which are very close to each other produces interesting repetition patterns with very long periods.

```
0100 PRINT "THIS PROGRAM DOES A VERY LONG, LONG DIVI-
     SION"
0110 INPUT "WHAT IS THE NUMBER TO BE DIVIDED? (THE
     NUMERATOR)" ,X
0120 INPUT "WHAT IS IT TO BE DIVIDED BY? (THE DENOMI-
     NATOR)" ,Y
0130 PRINT "HOW MANY DECIMAL PLACES SHOULD THE AN-
     SWER (THE QUOTIENT)"
0135 INPUT "BE CARRIED OUT TO" ,N
0140 GOSUB 1020
0150 GOTO 110
```

Listing 2: This is a demonstration program which will allow you to input any two integer values and have the result printed on an arbitrary precision.

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This is a 4K Z-80 machine language program utilizing every byte of available memory on the TRS-80. It displays a graphic chessboard and even flashes the piece on which the computer narrows its attention prior to making its move. Based on earlier chess programs for the 8080 and 6502 microprocessors, Microchess incorporates the improvements suggested by hundreds of users, and offers three levels of play to challenge all players from beginners to real chess enthusiasts.

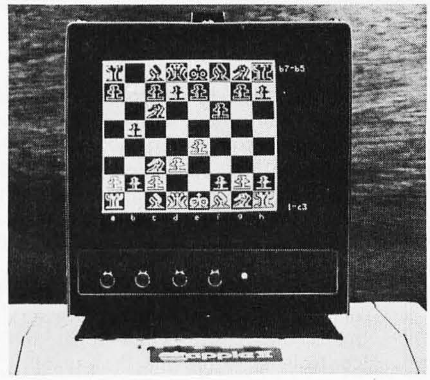
Microchess can be fun on any TRS-80 and is easily loaded from cassette with the CLOAD command. Standard algebraic notation is used to describe the moves, and a simple command lets you temporarily number the squares to assist in move entry. Every move is checked for legality, and the program even handles castling and en passant captures. You can play white or black, set up special board situations and play them out against the computer, or even watch the computer play against itself.

MICROCHESS 2.0 - for 8K PET's and 16K Apples

In 6502 machine language, this version of Microchess offers eight levels of play to suit everyone from beginner to the serious player. It examines positions as many as six moves ahead, and includes a chess clock for tournament play. $19.95 each.
TRS-80 (4K) ☐ PET (8K) ☐ Apple (16K) ☐

BRIDGE CHALLENGER — by George Duisman — from Personal Software™

If you like to play bridge but have trouble getting four people together to play, or if you'd just like to practice a little to improve your play, this program cassette is for you. With Bridge Challenger you and the dummy play against the computer in regular contract bridge. You can let the computer deal, or set up hands for study and practice play and save them on cassette. Created by George Duisman, an expert bridge player and programmer, this program takes full advantage of the PET's BASIC and requires all of the 8K RAM to run. Standard bridge notation, like that found in books and newspaper columns, is used to help you analyze the hands. Complete instructions, including an introduction to bridge for the novice, are included in six pages of documentation. $14.95 each.
TRS-80 (16K Level II) ☐ Pet (8K) ☐ Apple (16K) ☐



STIMULATING SIMULATIONS — by Dr. C. William Engel — from Personal Software™

This is a set of ten original simulation games written by Dr. Engel. The games are fun, and the 64 page paperback book which accompanies the cassette giving instructions, flowcharts, program listings and suggested modifications makes Stimulating Simulations an educational tool too. The games begin on an elementary level and progress to more complex problem situations, but most can be played by schoolchildren. The program listings in the book are in PET or TRS-80 Level II BASIC but special versions of the programs are provided for Level I BASIC users. $14.95 each.
TRS-80☐ PET ☐

...now!

GRAPHICS PACKAGE — from Personal Software™

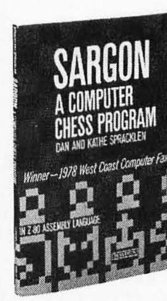
This set of four programs provides a quick and easy way for you to use your PET for several of the most common graphics applications: plotting equations or data, drawing pictures, and creating headlines of block letters. These programs, written by Dr. Peter Maggs, make use of the PET's graphic capabilities and can provide another dimension in your personal computing.
PET ☐

ASSEMBLER IN BASIC — from Personal Software™

Now you can write programs in assembly language for the 6502 microprocessor and have them translated to machine language for direct execution on your PET. The assembler accepts all standard 6502 mnemonics, pseudo-ops and addressing modes plus a new TEXT pseudo-op, and evaluates binary, octal, decimal, hexadecimal and character constants, symbols and expressions. You can create assembly source programs with the text editor which is supplied, and save them on cassette. The assembler reads its source code from cassette or from DATA statements, and assembles machine code directly at any location in memory. You can save machine language subroutines in the PET's second cassette, buffer, and execute them immediately with keyboard and display input/output. $24.95
PET ☐

ASTROLOGY PROGRAMS — by Michael Erlewine — from Personal Software™

You enter the date, time, and place of your birth. The program computes the sidereal time on the equator of your birth and your ascendant or rising sign, midheaven, and vertex angles in degrees / sign of zodiac / minutes of arc format. The helio and geocentric planetary positions are also given,and the program will optionally calculate and display the Local Space positions of the planets, the Local Space chart for a locality shift, give the position and direction in azimuth along the horizon of any city in the world, or display the equatorial coordinates for your natal planets. You can even input the right ascension and declination of any celestial object, and the program will compute its position on the horizon or Local Space chart. This program is loaded with celestial mechanics equations, and will save you or your astrologer hours of calculating time. $14.95
PET ☐



SARGON — A COMPUTER CHESS PROGRAM — by Dan and Kathe Spracklen — from Hayden

SARGON is the computer chess program that won the 78 West Coast Computer Faire tournament for microcomputers. Now you can run it on your own TRS-80 Level II. It is available in two forms: the book which contains the program listing in Z-80 assembly language and enough documentation to enable you to tailor and run it on your 8K Z-80 machine, and in cassette form ready to run on any TRS-80 Level II. Test your skill in this classic game; the machines are getting better!

Sargon Book with listing ☐ $14.95
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February 1-3, Future Fair, Memorial Coliseum, Portland OR. This northwest regional exposition will feature both professional and personal data processing products and services. Contact WES/COM, POB 4047, Portland OR 97208.

February 1-3, Microprocessor Programming Workshop with a Take-Home Microprocessor, Jefferson Plaza Building, Arlington VA. Sponsored by the IEEE, this 3 day workshop is intended for the practicing engineer, engineering manager and programmer. The course objective is to provide state of the art information in order to acquire an understanding of the place of microprocessors as replacements for wired logic and as controllers; to provide the capability of understanding the design of systems involving microprocessors; and the ability to program the Motorola M6800 microprocessor in machine language. All students will have their own microprocessor and laboratory equipment. Contact IEEE Service Center, 2145 Hoes Ln, Piscataway NJ 08854.

February 5-7, Data Processing Operations Management, Los Angeles CA. This seminar will emphasize the management skill and techniques applicable to the data processing operations function. The curriculum is designed toward practical, applied management techniques to provide a sounder understanding of the ways of managing data processing operations more effectively. For further information contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

February 13-15, The National Office Exhibition and Conference, Harbour Castle Hilton Convention Center, Toronto, Ontario. This 3 day exhibition will provide a showplace for approximately 100 exhibitors in the areas of word processing, office computers, office equipment and furniture. Contact Canadian Office Magazine, 2 Bloor St W, Suite 2504, Toronto, Ontario CANADA M4W 3E2, (416) 967-6200.

February 14-16, The IEEE International Solid-State Circuits Conference, Philadelphia PA. Forum for the presentation of new advancements in all aspects of solid-state circuits. Contact Lewis Winner, 301 Almeria Av, POB 343788, Coral Gables FL 33134.

February 19-21, Minicomputers and Distributed Processing, Chicago IL. This seminar will examine the uses, economics, programming, and implementation of minicomputers. Current hardware and software will also be evaluated. Contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

February 20-21, The Seventh Annual Midwest Digital Equipment Exhibit and Seminar, Thunderbird Motel, Minneapolis MN. Manufacturers of computer terminals, data communication equipment, peripherals, data acquisition systems, and digital test instruments will be displaying their products. In addition, appropriate seminars will be held every day. Contact Clarence K Peterson, Deerland Distributors Inc, Hennepin Square Bldg, Minneaplis MN 55413.

February 22-23, 1979 ACM Computer Science Conference and SIGCSE Symposium, Dayton Convention Ctr, Dayton OH. Several invited speakers will give full-length talks, and short current research papers will be presented. There will also be a technical symposium on computer science education held in conjunction with the conference. Contact Marshall Yovits, Computer and Information Science Dept, Ohio State University, Columbus OH 43210.

March 3-4, Micro-Expo '79, Texas A and M University Memorial Student Ctr, College Station TX. Sponsored by The Texas A and M Microcomputer Club, the activities at the third annual Micro-Expo '79 will include exhibits by dealers

and hobbyists, a programming contest, and a computer chess tournament, as well as seminars on topics of interest to both the novice and the experienced computer enthusiast. Contact Larry Brown at (713) 693-5748 or Scott Edwards at (713) 845-5531.

March 10-11, Personal Computer Fair, Pacific Science Ctr, Seattle WA. The fair will acquaint people with personal, home and hobby computer applications. Visitors will see a variety of nontechnical demonstrations and have numerous opportunities for hands-on experimentation. Contact Susan Stocker, Pacific Science Ctr, 200 Second Av N, Seattle WA 98109.

March 19-20, Microcomputers: Operating Principles, Hardware and Software Seminar, Holiday Inn, Palo Alto CA. Polytechnic Institute of New York and the Institute for Advanced Professional Studies are presenting this 2 day seminar for engineers, programmers, and technical managers involved with selection of microprocessors and design of microprocessor-based systems. The seminar will cover the underlying concepts governing microprocessor operation, architecture, and systems design. Microcomputer elements and their interrelationships will be discussed, emphasizing features important in determining whether a particular microcomputer will be suitable for a given task. Contact Prof Donald D French, Institute for Advanced Professional Studies, 1 Gateway Ctr, Newton MA 02158, (617) 964-1412.

March 19-21, Project Management for Computer Systems, Atlanta GA. This seminar is designed for the computer oriented professional responsible for the development and implementation of complex EDP systems. The seminar will illustrate techniques for planning, implementing, installing, and controlling projects. Contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

March 19-21, Federal DP Expo Conference and Exposition, Sheraton Park Hotel, Washington DC. This fifth annual government show will feature computer related hardware, software and service.

March 19-21, Modern Integrated Circuits, George Washington University, Washington DC. This course is structured to meet the needs of engineers, scientists, and technical managers who desire a better understanding of the latest technological advances in the area of integrated circuits. As such it examines all aspects of integrated circuit technology, starting from fundamental principles of construction and operation, to the most recent devices, their characteristics and specifications. A significant part of the course deals with the application of integrated circuits in linear and digital systems. Specific topics to be covered include detailed design examples of circuits using operational amplifiers and active filters, as well as computer arithmetic units, registers, and memories. Contact George Washington University, Continuing Engineering Education Program, Washington DC 20052.

March 21-23, Microcomputer Hardware and System Design Seminar, Holiday Inn, Palo Alto CA. Polytechnic Institute of New York and the Institute for Advanced Professional Studies are presenting this 3 day seminar for engineers, programmers and technical managers with a working knowledge of digital hardware design and familiarity with the underlying concepts governing microprocessor operation, architecture, and systems design. This seminar will cover the operation, architecture, instruction set, and design techniques for 8 bit microprocessors. The spectrum of applications from data processing to control will be illustrated with fully developed case studies. Contact Prof Donald D French, Institute for Advanced Professional Studies, 1 Gateway Ctr, Newton MA 02158, (617) 964-1412.

March 25-28, Expo '79 Los Angeles Marriott, Los Angeles CA. Expo '79 is held in conjunction with the 16th Numerical Control Society Annual Meeting and Technical Conference. Contact Numerical Control Society, 1800 Pickwick Av, Glenview IL 60025, (312) 724-7700.

March 26-28, Data Processing Operations Management, Houston TX. See February 5-7, Los Angeles CA.

March 26-28, Minicomputers and Distirbuted Processing, New York NY. This seminar will examine the uses, economics, programming and implementation of minicomputers. Current hardware and software will also be evaluated. Contact The University of Chicago, Center for Continuing Education, 1307 E 60th St, Chicago IL 60637.

March 27-29, The Midwestern Computer Expo, McCormick Pl, Chicago IL. Exposition by the leading vendors of data processing equipment and services. Contact Lee Mulder, The Caravan Group, 60 Austin St, Newton MA, (617) 964-4550.

April 3-5, Specifications of Reliable Software, Hyatt Regency Hotel, Cambridge MA. This conference is sponsored by the IEEE Computer Society. Contact

Douglas T Ross, Softech Inc, 460 Totten Pond Rd, Waltham MA 02154, (617) 890-6900.

April 5-6, Computers in Ophthalmology, St Louis MO. This is a course in application of computers to ophthalmic patient care and clinical reseach. Sessions dealing with data bases, automated patient testing, artificial intelligence, and image processing are being planned. Contact Robert Greenfield, DSc, Biomedical Computer Laboratory, Washington University School of Medicine, 700 S Euclid Av, St Louis MO 63110.

April 6-8, Northeast Personal and Business Computer Show, Hynes Auditorium, Boston MA. Displays and exhibits will showcase microcomputers and small computer systems of interest to businesspeople, hobbyists, professionals, etc. Lectures and seminars will be presented for all categories and levels of enthusiasts, including introductory classes for novices.

April 9-11, Data Processing Operations Management, Miami FL. See February 5-7, Los Angeles CA.

April 9-12, Interface '79, McCormick Pl, Chicago IL. This is the seventh annual conference and exposition on data communications and computers. Contact The Interface Group, 160 Speen St, Framingham MA 01701.

April 16-20, Data Communication Systems and Networks, George Washington University, Washington DC. This course is designed for systems analysts, engineers, managers, and others who need a better working knowledge of data communication systems. The course will be of particular value to those who are currently planning, designing or implementing a computer that involves data communications. The objective of the course is to provide participants with an understanding of the basic principles and current techniques involved in computer to computer and terminal to computer communications and networking. Contact Continuing Engineering Education, George Washington University, Washington DC. 20052.

April 23-26, Middle Eastern Electronic Communications Show and Conference, Bahrain Exhibition Ctr, Bahrain. The exhibition will consist of companies marketing communication systems, products, and services. Contact Gerry Dobson, MECOM '79, Arabian Exhibition Management, 11 Manchester Sq, London W1M 5AB.

April 24-26, Electro/79 Show and Convention, New York Coliseum and American Hotel. Contact William C Weber Jr, general manager, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo CA 90245.■

___ **Microcomputer Problem Solving Using PASCAL** by Kenneth L Bowles. This book is designed both for introductory courses in computer problem solving at the freshman and sophomore college level, and for individual self-study. Graphics is stressed in this version of the book, in many cases borrowing from the "Turtle Graphics" approach originated by Seymour Papert of MIT. A complete single-user software system based on PASCAL has been developed at the University of California at San Diego, where the author is a professor in the Department of Applied Physics and Information Science. This system embodies extensions to the standard PASCAL which include the necessary functions and procedures for handling graphics and strings. 563 pp. $9.80.

___ **An Introduction to Programming and Problem Solving With PASCAL** by G M Schneider, S Weingart, and D Perlman. This book has three major goals:

(1) To introduce *all* aspects of the programming and problem solving process, including problem specification and organization, algorithms, coding, debugging, testing, documentation, and maintenance.
(2) To teach good programming style and how to produce a high quality finished product. This is brought out in numerous style examples throughout the text.
(3) To teach the syntax of the PASCAL programming language.

PASCAL is used as a vehicle to teach various aspects of programming techniques. $13.95.



Speaking of PASCAL . . .

___ **PASCAL User Manual and Report** (Second Edition) by K Jensen and N Wirth consists of two parts: the User Manual and the Revised Report. The Manual is directed to those who have some familiarity with computer programming and who wish to get acquainted with the PASCAL language. It is mainly tutorial and includes many helpful examples to demonstrate the various features of the language. The Report is a concise reference for both programmers and implementors. It defines Standard PASCAL, which constitutes a common base between various implementations of the language. $7.90.

___ **Programming in PASCAL** by Peter Grogono. This book is an excellent introduction to one of the fastest growing programming languages. The text is arranged as a tutorial containing both examples and exercises to increase reader proficiency in PASCAL. Besides sections on procedures and files, there is a chapter on dynamic data structures such as trees and linked lists. These concepts are put to use in an example bus service simulation. Other examples range from the Tower of Hanoi problem to circumscribing a circle about a triangle. **Programming in PASCAL** is sure to hold the reader's interest. 359 pp. $9.95.

___ **The Design of Well-structured and Correct Programs** by S Alagic and M A Arbib. This book represents ten years of research in top-down program design and verification of program correctness, and demonstrates how these techniques can be used in day-to-day programming with PASCAL. An explanation of control and data structures and many examples of programs and proof development are provided. As a programming text, this book contains an introduction to the language, provides algorithms which operate on sophisticated data structures, and offers the full axiomatic definition of PASCAL in terms of proof rules. To use this book, no particular mathematical background is necessary beyond the basic idea of a mathematical proof, although an introductory course in programming is required. 292 pp. $12.80.

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Build a Computer Controlled Security System for Your Home: Part 2

Ciarcia's Circuit Cellar

Steve Ciarcia
POB 582
Glastonbury CT 06033

"Hi, Lloyd. What brings you over this afternoon?" Lloyd often came over unannounced, so I wasn't surprised. I barely lifted my eyes from the circuit I was inspecting as he approached.

"I just wanted to see how the security system was coming. I brought along the telephone number of the alarm company that did my house, should you care to reconsider and be more conventional."

"It's more fun this way," I responded.

"I just about made it into the driveway out there. It's like Grand Central Station. What's going on?"

"You can't have remotely controlled perimeter lighting without installing floodlights." There were two electricians wiring eight sets of high intensity floodlights to a central control panel in the basement (see photo 1). This control panel in turn would be connected to the computer for automatic control of the lights. "Besides those are high intensity 250 W lights. With three or four of them on a circuit, they had better be wired correctly."

"Electricians? Floodlights? Wouldn't it be cheaper to wire it yourself?"

"When you install this kind of system, you have to be extremely careful not to create a problem greater than the one you're trying to alleviate. Outside weatherproof cabling isn't exactly my bag. I'd much rather sit here and make the modifications to the SDK-85 controller. Sit down and I'll explain what has to be done."



Photo 1: View of author's house. Professional electrician Russ Molitoris is shown stringing electrical conduit pipe for high intensity outside lighting. Conduit from all external lights runs to central control panel in basement which accepts DC on/off control commands from the computer. Conduit is used to meet electrical code requirements.

SDK-85 Modifications

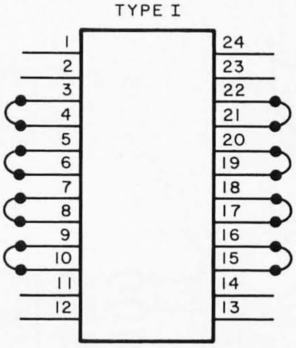
The program necessary for this application requires slightly under 1 K bytes of memory. Since the control algorithms are fixed and do not change, they should be written in nonvolatile storage of some kind. For our purposes an ultraviolet erasable read only memory such as a 2708 or 2716 is recommended. As supplied, the SDK-85 contains 256 bytes of programmable memory used by the control program for stack storage and variable tables. While 256 bytes is adequate once the system is operational, additional programmable memory is suggested for checkout purposes. The larger area allows room for multiple diagnostic subroutines. Once checkout is completed, the 1 K byte memory buffer can be removed and the software readdressed to the location of the 256 byte buffer. This is not a requirement, however.

There are two ways to add additional erasable read only memory to the SDK-85. The simplest is to buy an 8755 2 K byte integrated circuit and plug it directly into the slot already provided for extra memory on the board (this slot can accommodate an 8355 read only memory or 8755 erasable read only memory). In industrial applications where the latest chips on the market are no problem to obtain, this is the only reasonable approach. For the computer experimenter, however, these parts are relatively hard to find, and the second approach must be investigated.

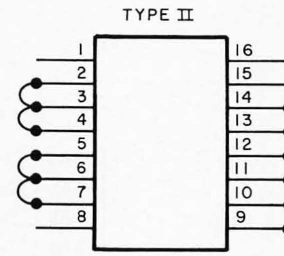
The 8085 differs from the 8080 in its method of multiplexing bus information to peripheral circuits. The new exotic large scale integration circuits like the 8755 incorporate full decoding logic which minimizes external support circuit requirements. Using the 8085, a complete computer with central processor, read only memory, programmable memory and I/O can be constructed with three integrated circuits. The addressing of these multifunction support circuits differs from the common variety of memory and I/O devices we have become familiar with. To use devices other than the 8755 and 8155 generation requires a series of demultiplexing registers and buffer drivers to break out the address and data lines to a logical equivalent to the 8080. The SDK-85 allows for optional bus expansion and provides nine blank, prewired integrated circuit locations for just this purpose.

Some of these registers and bus drivers are relatively expensive considering our requirements. With the nine integrated circuits inserted, a full 65 K bytes of expansion memory can be accommodated. The additional 1 K bytes required in the present application does not warrant this much expense. The method illustrated for expanding the memory of the SDK-85 using readily available components is predicated on its staying a small system, ie: less than 8 K bytes. The full expansion circuitry is required above this value. Table 1 shows the necessary modifications.

Photo 2 is a close-up of the header



TYPE	*AT LOCATION*	*FOR*
I	A1	HIGH ADDRESS
II	A4	HIGH DATA
II	A7	LOW DATA
II	A2, A5, A3	CONTROL



Modifications to SDK-85 Board
(for small system)

Note: An Intel (single 5 V supply) 2716 can be substituted by removing the −5 and +12 V supply connections and tying pin 19 to BA10. (Numbers with J prefixes refer to connector pins on the SDK-85 board. Numbers with A prefixes are integrated circuit locations.)

- Solder in 40 pin wire wrap headers at J1 and J2.
- Solder in 34 pin wire wrap headers at J3.
- Solder in 26 pin wire wrap headers at J4 and J5. (I used Scotchflex wire wrap headers.)
- Insert 8212 at A6 to hold low address lines mutliplexed.
- Insert jumper headers as in table 1.
- Add 74S00 at A8 and 74LS74 at A9 to enable line DSI 8212 (except during HOLD). Other buses are unbuffered, and will be floated at 8085.
- Meaning of signals on J1 and J2 remains the same as with SDK-85 circuitry, just less drive level for a small system.
- Now add standard 8080 I/O memory devices via J1 and J2 wire wrap posts.

Table 1: Modifications which must be made to the SDK-85 board to expand the memory capabilities.

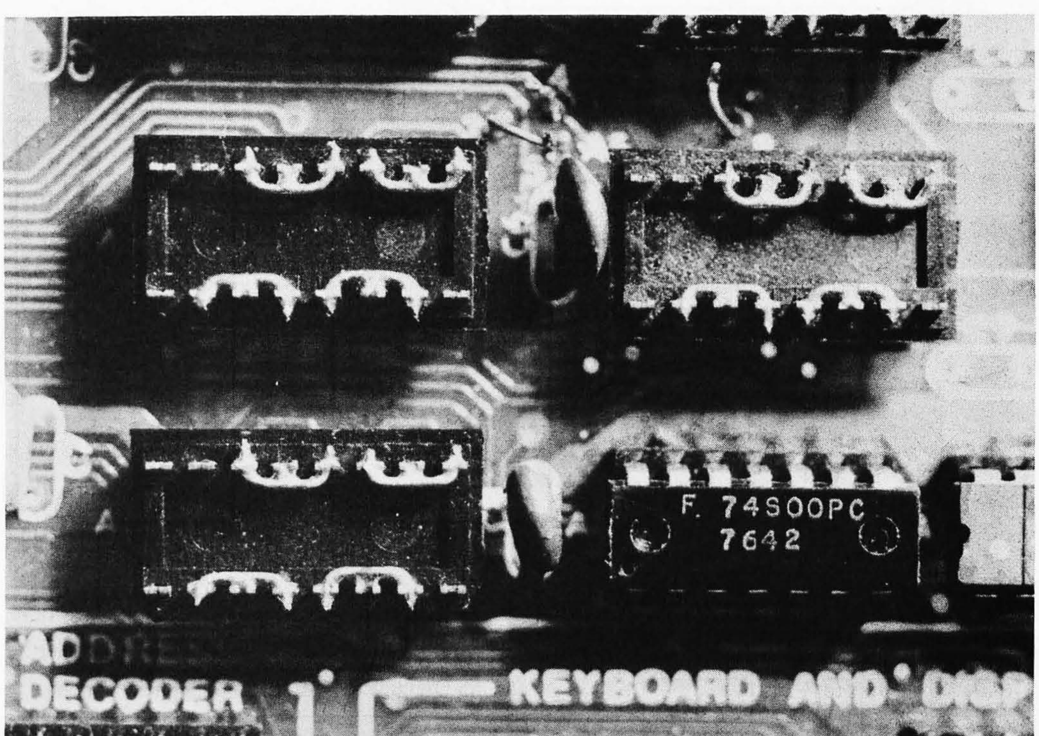


Photo 2: To add the additional memory to the SDK-85, nine integrated circuits are required. If a limited quantity of expansion is required, the technique described in the text using three integrated circuits and jumpers can be used. This photo illustrates these jumper headers installed in the circuit.

Software consulting for this series of articles was provided by Steve Sunderland.

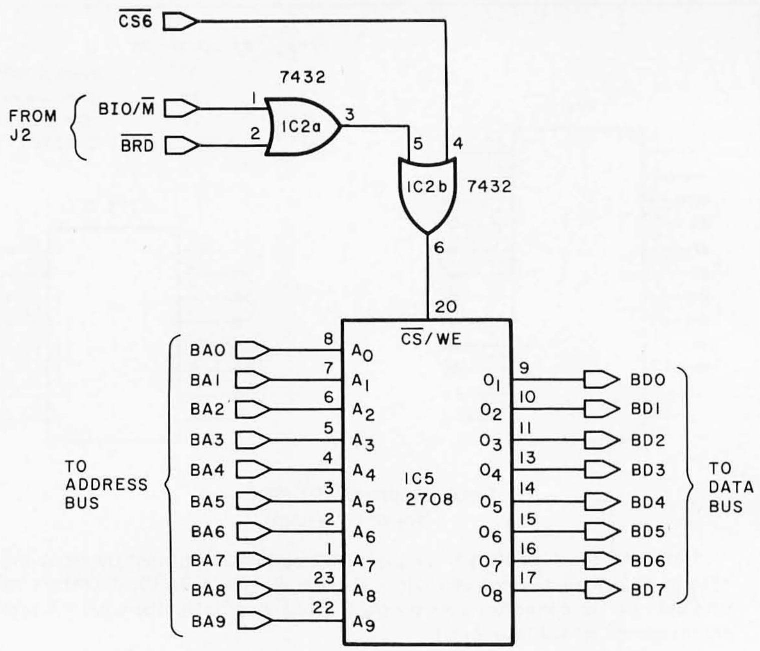


Figure 1: Circuit for adding a 2708 erasable read only memory to the SDK-85 computer board. Note that an Intel 2716 (single 5 V supply) can be substituted by removing the −5 V and +12 V power supply connections and tying pin 19 to BA10.

jumpers installed in the appropriate sockets on the board. Figure 1 illustrates the circuit connections for adding a 2708 to the basic board once the address lines have been brought out. Similarly, figure 2 details the circuit for adding 1 K bytes of programmable memory. The suggested placement of these components is in the prototype assembly area provided on the board. Photo 3 demonstrates a viable placement and photo 4 shows how much wiring will be required to make these modifications.

If wired as described, the system memory will be mapped as in table 2.

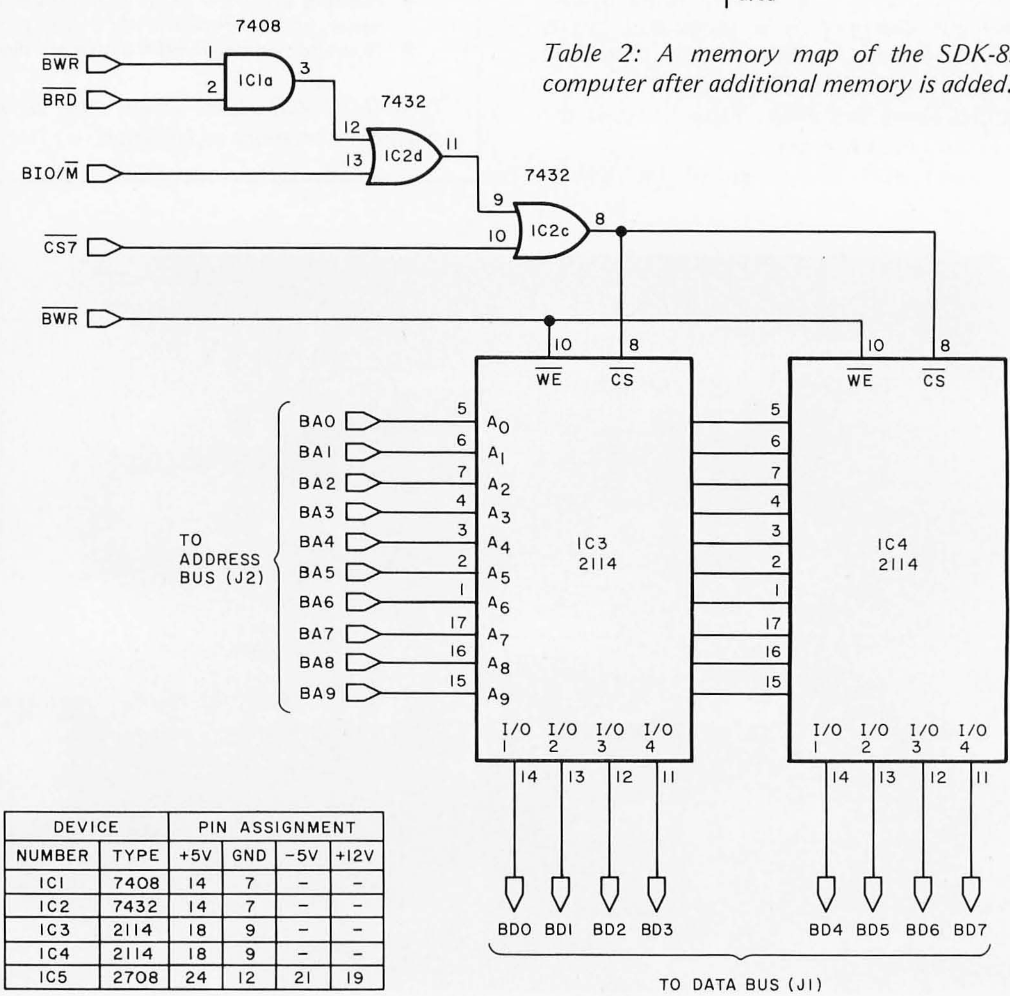
Computer Software

As stated in the first article in this series,

Hexadecimal Memory Location	Description
2000 thru 20FF	original on board programmable memory
3800 thru 3C00	1 K byte programmable memory expansion
0000 thru 07FF	2 K byte read only memory monitor
3000 thru 3400	read only memory expansion area

Table 2: A memory map of the SDK-85 computer after additional memory is added.

Figure 2: Circuit for adding 1 K bytes of programmable memory to the SDK-85 computer.



DEVICE		PIN ASSIGNMENT			
NUMBER	TYPE	+5V	GND	−5V	+12V
IC1	7408	14	7	–	–
IC2	7432	14	7	–	–
IC3	2114	18	9	–	–
IC4	2114	18	9	–	–
IC5	2708	24	12	21	19

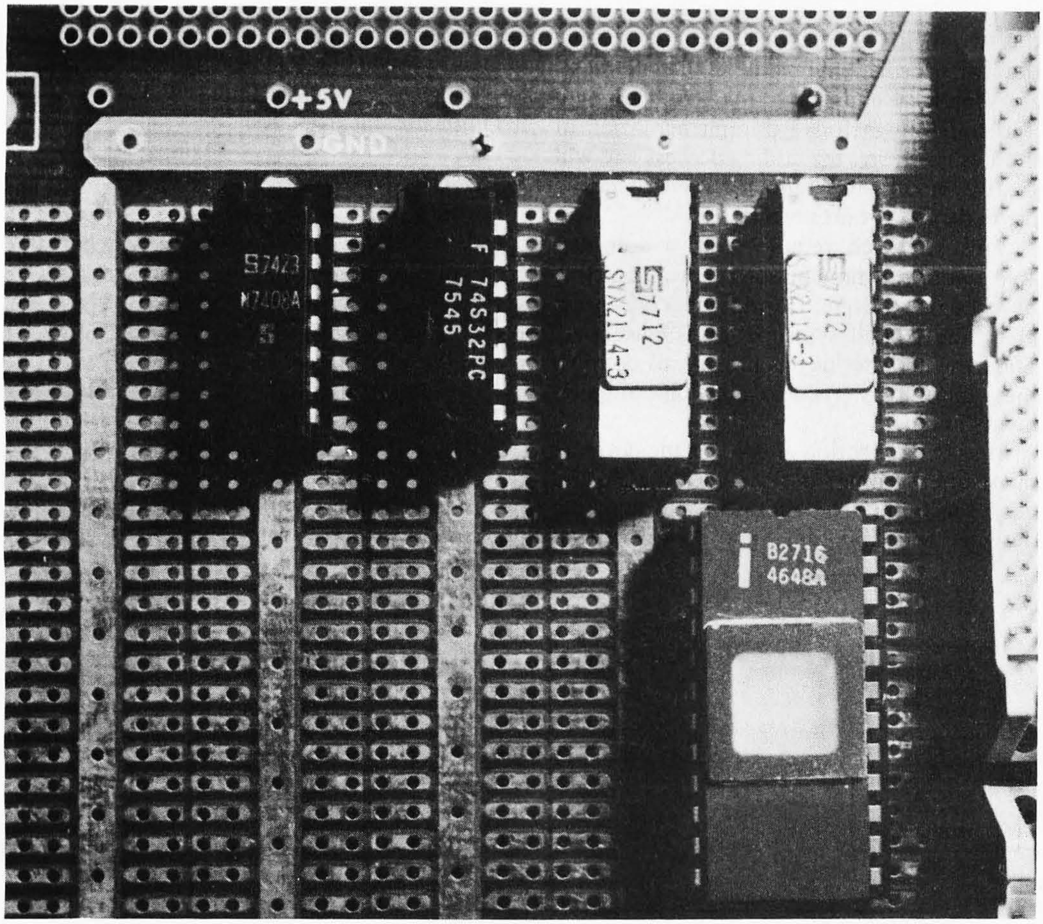
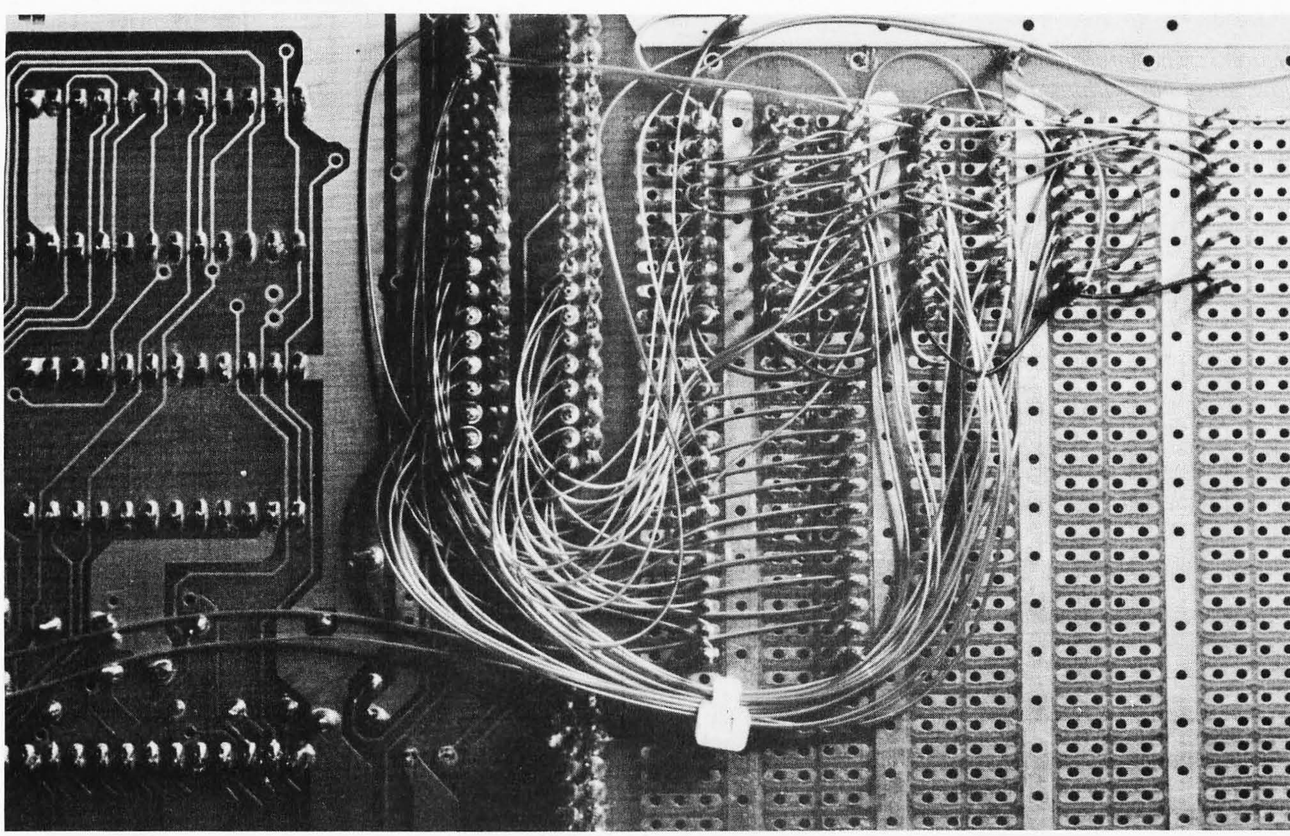


Photo 3: Left side of the SDK-85 board contains a prototyping area which, in this case, has been used for the extra memory circuitry. The photo shows an Intel 2716 2 K byte erasable read only memory which was used because of a desire for single supply power backup. The software only requires 1 K bytes and can use a 2708 instead. Scotchflex connectors to the right of the 2114 and 2716 attach the SDK-85 to the external sensor inputs and control output.

Photo 4: Attachment of additional memory can be easily done using wire wrap techniques. This photo demonstrates the complexity of the connections.



the two major factors involved in developing the software for the home security system are simplicity and flexibility. Simplicity will lead to a straightforward implementation of the design during the coding process and will greatly reduce the time required to debug the code and get on the air.

This approach requires that a considerable amount of time be spent before one line of code is written. During the conceptual phase, an overall system logic is developed. Then the designer begins the task of defining the tables, files, records and logic requirements in detail.

Iterative reflection allows for the development of a "simple" design which is clear and easy for others to follow. In addition, the designer will find that upon completion of this process, the various software modules will have virtually coded themselves, greatly reducing the time required to code and implement a given design.

System Overview

Figure 3 illustrates the flow of information in this security system.

The cold start procedure causes the system to initialize the sensor state transfer table, delay timer file and time of day file. This procedure requires time of day entry through the keyboard in hours and minutes (24 hour clock) so that the system will be able to activate events in the proper sequence. Upon completion of this procedure the cold start initializes the digital input or

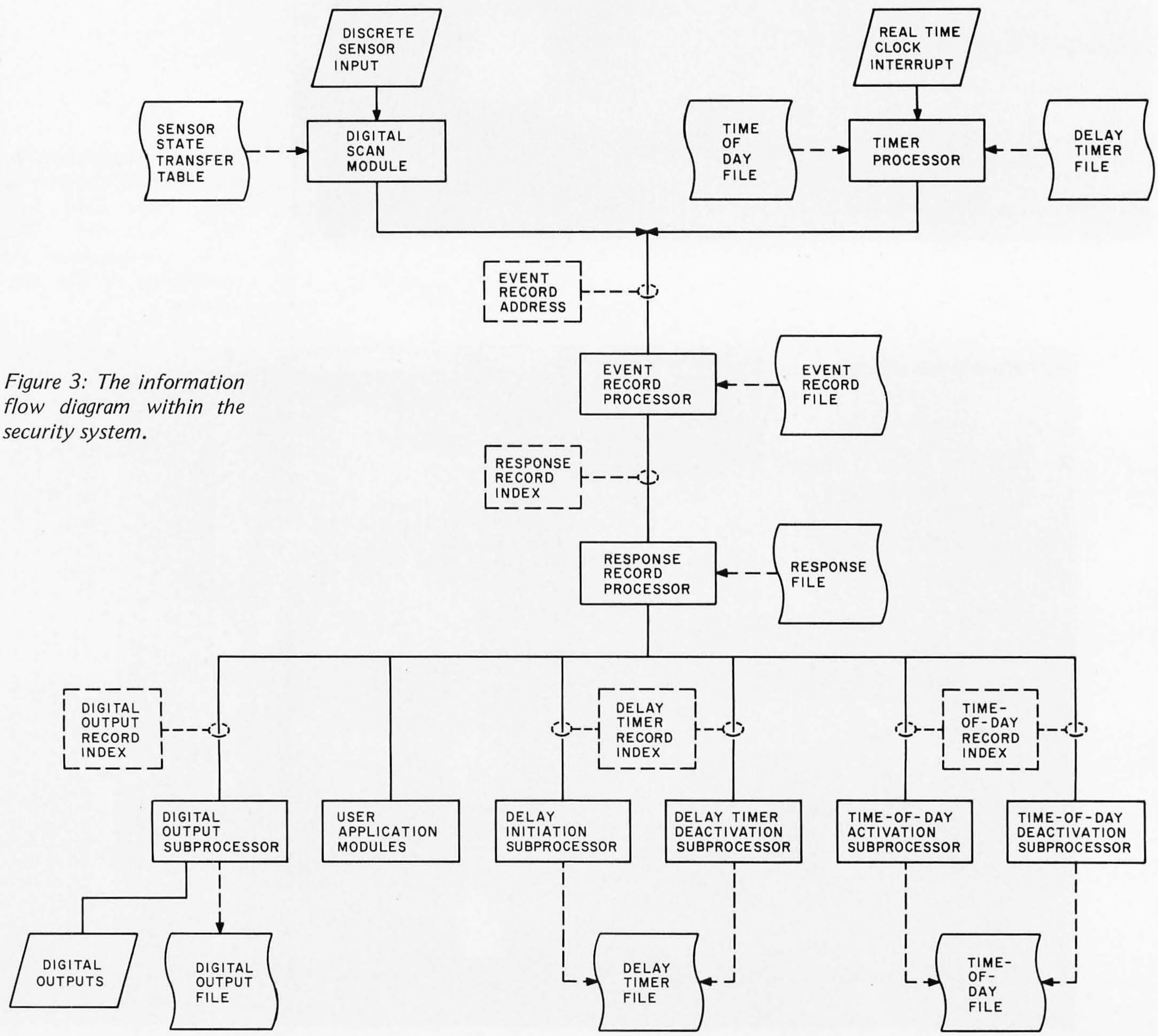


Figure 3: The information flow diagram within the security system.

sensor states, activates the real time clock interrupt, and starts scanning the sensors. (Intruders beware, for the security system is now active!)

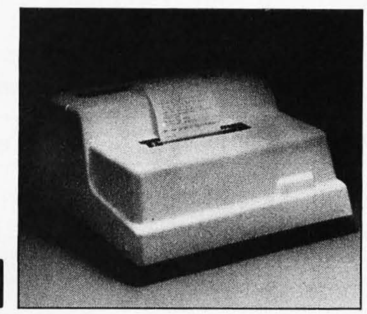
The system continually monitors the state of the various sensors via the digital scan module; and periodically (once a second) checks to see if any time events are to be initiated. In order to demonstrate how a timed event function is processed, let's assume that one of the time of day records initiates the sequence that tells the system to turn the percolator on at 0600. As the system processes each interrupt from the real time clock, the time in this record will be compared to the current time of day. When they are equal, the events leading to a freshly brewed cup of coffee would be under way.

The first step in this example is effected by the timer processor which extracts an event record address from the time of day record and passes it to the event record processor. The event record processor assumes control, and using the record address passed to it, obtains from the event record file the list of response records to be processed for this event.

Only one response record is required. However, for more complex functions the event record can be structured to execute up to 255 different responses to an event. The response record index, which the event record processor obtains from the event record, is now transferred to the response record processor.

The response record processor, using the index supplied, obtains a record from the response file. In our example this record directs the processor to activate the digital output subprocessor and passes the index of the digital output record to be used in turning on the percolator. Having accomplished this function the subprocessor returns control to the event record processor, which checks to determine if any further responses are required. If so, it will initiate the response. In our example no further response is required and control is returned to the timer processor. This completes processing of those delay and time of day records requiring servicing. This same procedure is used in the servicing of delay timer records whose delay time has expired.

The servicing of a sensor event is initiated by a different mechanism. However, once control is transferred to the event record processor the servicing of the event follows the same sequence as our percolator example. The event record processor will return control to the digital scan module when it completes initiation of all the responses associated with the event.



To illustrate the processing of a sensor detected event, let's assume that you have installed a photodetector at the entrance to your driveway. When this sensor is activated, an exterior light in your home is to be turned on.

The digital scan module is continually scanning the state of the sensors connected to the input ports of the security system. When this module detects that the photoelectric device has been tripped, the sequence that turns on the light is initiated. Using the information it has, the scan module obtains from the sensor state transfer table the record associated with the driveway sensor. This record contains two entries: one for the sensor going to a set (1) state, and one for a reset (0) state. These two entries are provided so that event processing can be initiated on a transfer to a set state, a transfer to a reset state, or both.

Assuming that a reset state triggers an event, the light beam is broken and the signal goes to a logic 0. The digital scan module extracts from the sensor state transfer table the address of the event record to be processed and transfers control to the event record processor. This results in the turning on of the exterior light.

These two examples should illustrate the manner in which the software modules interact with one another. A detailed description of the functions of each module and the structure of the various records, tables and files used in the system follows.

Cold Start

The cold start module requires some special tailoring for each system. It is the responsibility of this module to start the operation of the system.

There are a few basic functions which this module must perform (see figure 4). The primary functions are to transfer the state transfer vector table, time of day file and delay time file from erasable read only memory to a preset location in programmable memory. The records in these files and tables contain volatile fields (data which will be periodically updated).

Another major function of the cold start module is obtaining the current time of day from the person initiating the system. The user enters this data via the keyboard located on the SDK-85 printed circuit board. (The SDK-85 is a good choice for this system because it provides the basic requirements for data entry and display.) The time of day as entered is displayed on the 6 digit LEDs and updated periodically by the real time clock.

The two remaining functions necessary

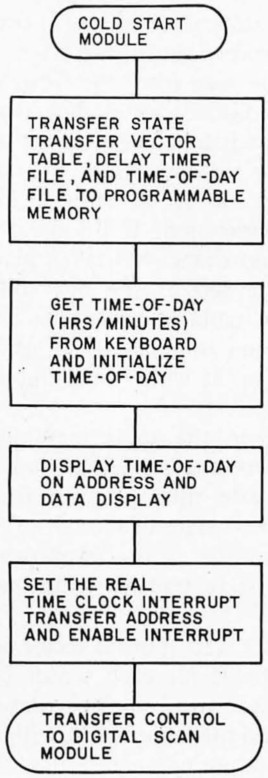


Figure 4: Cold start logic module.

to the cold start process are the initiation of the digital input state table and enabling of the real time clock interrupt. The detection of a digital event is the result of a comparison of the current state of a digital output with its previous state. Therefore, the initial state must be explicitly set. The state table for all digital or sensor inputs resides in volatile memory and must be set to zero to avoid ambiguity caused by powering up the system.

Since the SDK-85 provides the user with a vectored interrupt capability, the final function of the cold start module is to set the final timer (user vectored interrupt) vector address. This is accomplished by placing a jump instruction at a previously defined address followed by the address of the real time clock interrupt module, ie: JP RTC + JUMP TO REAL TIME CLOCK.

After initiating the interrupt transfer address, the cold start module enables the real time clock interrupt and transfers control to the digital scan module.

Digital Scan Module

The responsibility for detecting an intruder, fire, smoke, etc, lies with the digital scan module. This module continually monitors the state of the digital sensor inputs and when it detects that an input has changed state (gone from a set (1) to a reset (0) con-

dition, or a reset (0) to a set (1) condition), initiates the processing of the event.

As can be seen from the flowchart (figure 5), the digital scan module reinitializes itself after each scan. As it scans the current status of the system sensors, the input data is compared bit by bit until all input bits have been processed. If the module determines that no change has taken place in the state of the sensor, the next bit in the sensor state table is processed. This function continues until all sensor states have been checked, at which time the process is started over.

If, however, the above mentioned technique detects that a sensor has changed state, the state history table is updated to reflect the new state of the sensor. The sensor state transfer record is extracted from the sensor state transfer vector table (see table 3).

The sensor state transfer vector table contains two fields for each sensor or digital input. These two entries comprise one record within the table or file, with each digital input requiring one record. The first entry or field within a sensor record contains the event record address to be passed to the event record processor upon a transition to a set (1) condition by the sensor, and the active/inactive flag (bit 7 of the upper address byte). The second field or entry contains the same information as the first, but is used when a transition to a reset (0) condition has taken place. If the active/inactive flag is reset (0) the entry is considered to be active and further processing may take place; if the flag is set (1) no further processing is allowed.

In the event that the sensor has undergone a transition to a set (1) condition, the first entry of the sensors state transfer vector record is obtained from the table, else the second entry is obtained. Then the active flag is examined. If this flag is found to be reset (0), the event record address is transferred to the event record processor for additional processing.

However, if the flag indicates the entry is inactive (flag equals 1), no further processing of the transition event will take place and the digital scan module will continue to process inputs in its normal manner.

As you may have noticed, the manner in which inputs are processed to completion is sequential in nature. That is, when a transition of a sensor requires processing, all processing associated with that event is completed before the next sensor input is processed. This is possible because the processing of a given event will not substantially delay the processing of the next sensor, since no appreciable I/O processing is required. One

other feature afforded by this design is that one or more sensors may use the same event record since after the digital input processing there is no further need to maintain the identity of the sensor undergoing the transition.

Since the processing of all inputs is sequential, the user should not incorporate lengthy input or output procedures in a user supplied application module.

Event Record Processor Module

As stated in the digital scan module description, the event record processor is activated when the digital scan module detects a state transition which requires processing. This module is also activated when an active delay timer (see timer interrupt processor module) or time of day event occurs.

Table 3: Sensor state transfer vector table format.

	Byte	Description
Record 1	0-1	Event Record Address for RESET to SET State Transfer for Digital Input 1 (High Order Bit=Active Flag)
	2-3	Event Record Address for SET to RESET State Transfer for Digital Input 1 (High Order Bit=Active Flag)
Record n	3-4	Event Record Address for RESET to SET Transfer for Digital Input 2 (High Order Bit=Active Flag)
	5-6	Event Record Address for SET to RESET Transfer for Digital Input 2 (High Order Bit=Active Flag)
	*	
	*	
	*	
Record n	(2n−1)–2n	Event Record Address for RESET to SET State Transfer for Digital Input n (High Order Bit=Active Flag)
	(2n+1)–(2n+2)	Event Record Address for SET to RESET State Transfer for Digital Input n (High Order Bit=Active Flag)

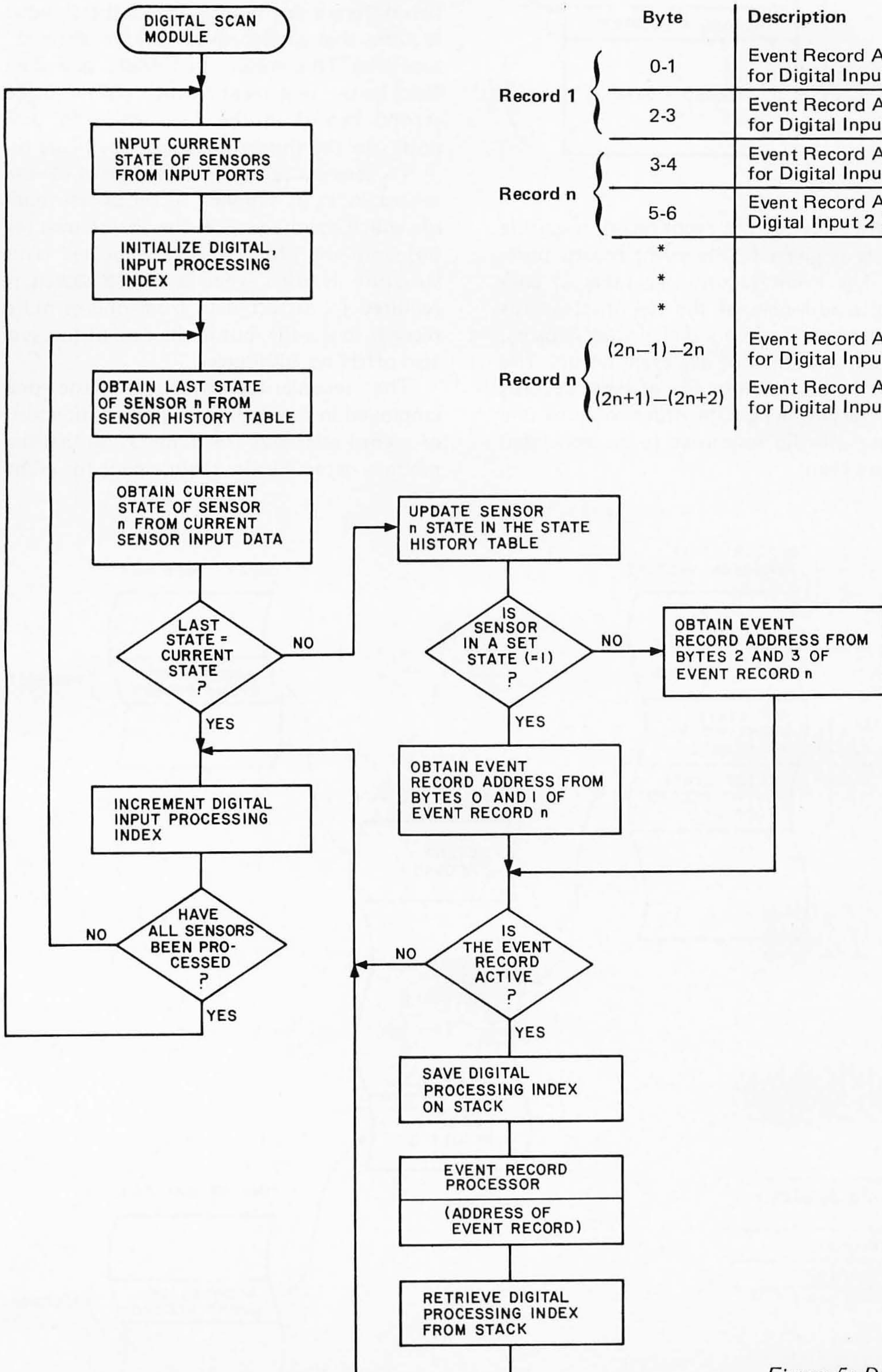


Figure 5: Digital scan logic design.

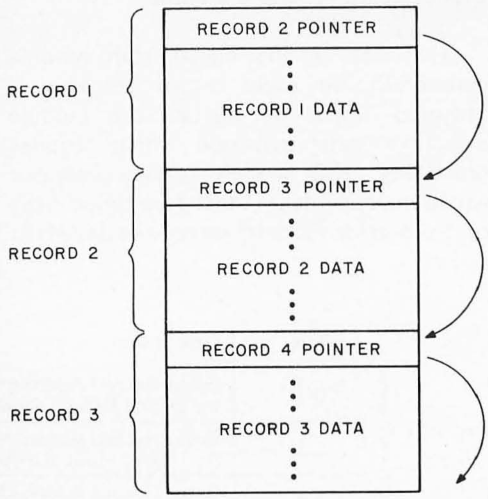


Figure 6: Representation of chained records in memory space.

The address of the event record requiring servicing is given to the event record processor. The event record (see table 4) contains the addresses of the response records to be processed when a digital scan (sensor), delay timer or time of day event occurs. The records in the table or file of event records are of varying length in order to allow one or more specific responses to be associated with any event.

This structure of the event record dictates the manner in which the record being processed must be accessed. Generally all records within a file are of fixed length and can be referenced by an index which serves as a relative pointer into the file to access the record in question. However, when the records within a file are of variable length, an absolute or relative address must be provided to obtain access to the record in question. This address may be obtained via two different techniques. The first technique requires that all records in a file be "chained" together. This means that there is a data field in the first record which points to the second record in the file, which in turn points to the third record, etc (see figure 6).

To access a record in this type of file the record index is supplied to the access module which then sequences the chain down (or up) until the proper record is located. This structure is used when a record search is required to extract data from one or more records in the file, but in the case of this system offers no advantages.

The second technique, and the one employed in this system, requires a directory of record addresses (see table 3), so that the module detecting the requirement for event

Figure 7: Event records are accessed through sensor state transfer vectors.

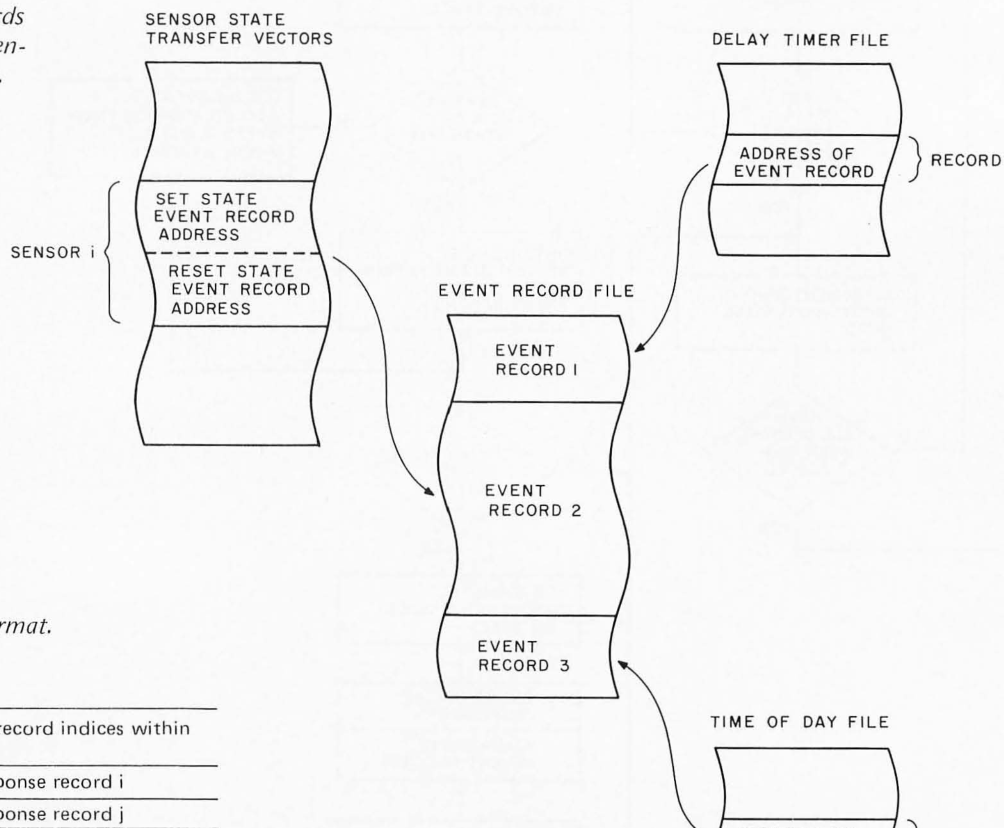


Table 4: Event record format.

Byte	Description
0	Number of response record indices within the record
1	Relative index of response record i
2	Relative index of response record j
* * *	
n	Relative index of response record z

processing will have access to the event record associated with the event (see tables 7 and 8) as is done with the timer delay and time of day records. An event record can therefore be isolated via one of three sources in the security system: the sensor state transfer vector table, the time of day records and the delay records (see figure 7).

Since an event record may contain more than one response directive, the first data field (byte 0) of the record contains the number of response records (see table 5) associated with the event in question. Those fields following within the record contain the relative indices of the response records that require processing.

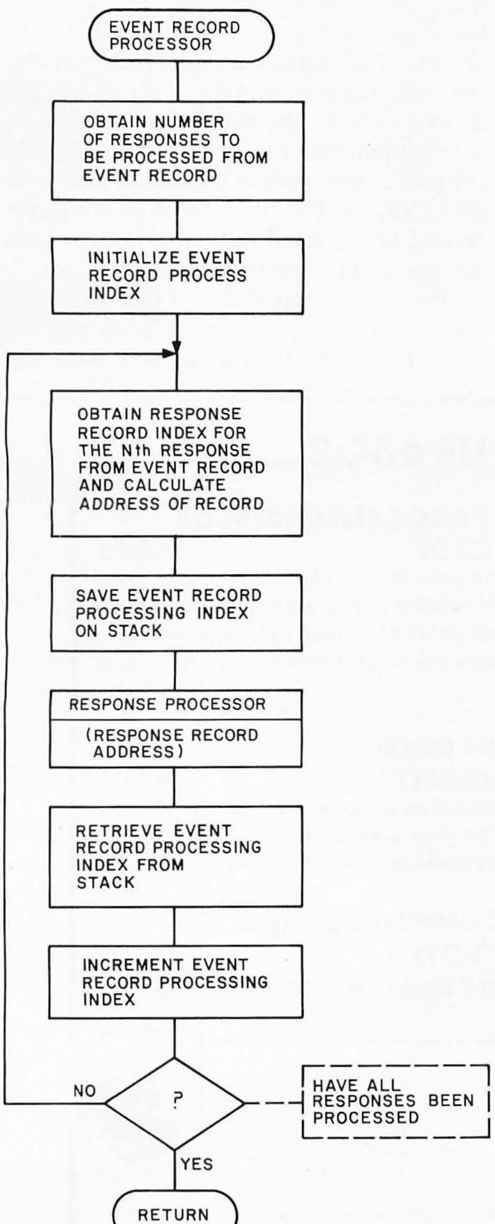


Figure 8: Event record processor logic diagram.

Upon entry, the module saves the event record address in a temporary working area and then extracts from the event record the number of response records to be processed (see figure 8). This data will then be used to initialize the event record processor counter and the initial response record address will be calculated:

Response Record Address =
(Response Record Index−1)x3
+ Base address of Response Record File

This response record address is then passed to the response processor for execution. When completed, control is returned to the event record processor. If additional records require processing, the next effective response record address is calculated and control is transferred to the response record processor. If all records have been processed, control is returned to the module initiating the request for service, either the digital scan module or the timer interrupt module.

Response Record Processor

The function of the response record processor (figure 9) is to determine from the response record the type of action required, and to activate the appropriate response subprocessor. The activated subprocessor will effect the final response and then return control to the event record processor.

There are six basic responses associated with an event. These responses are defined by the response record (table 5) and are:

- Activation of a digital output
- Execution of an application module
- Initiation of a delay timer
- Deactivation of a delay timer
- Activation of a time of day record
- Deactivation of a time of day record

The user should be aware of the function of each subprocessor and certain idiosyncrasies. The processing of a digital output is the function of the output subprocessor. This processor will, upon activation, receive from the response processor the index of the digital output record (table 6) it is to process. The digital output record contains the information necessary to effect the desired output. The current output state of each output bit of the port is maintained in the port's state word in the output port state file. Each set (1) bit in the state word represents an activated output, and each reset bit represents a deactivated output.

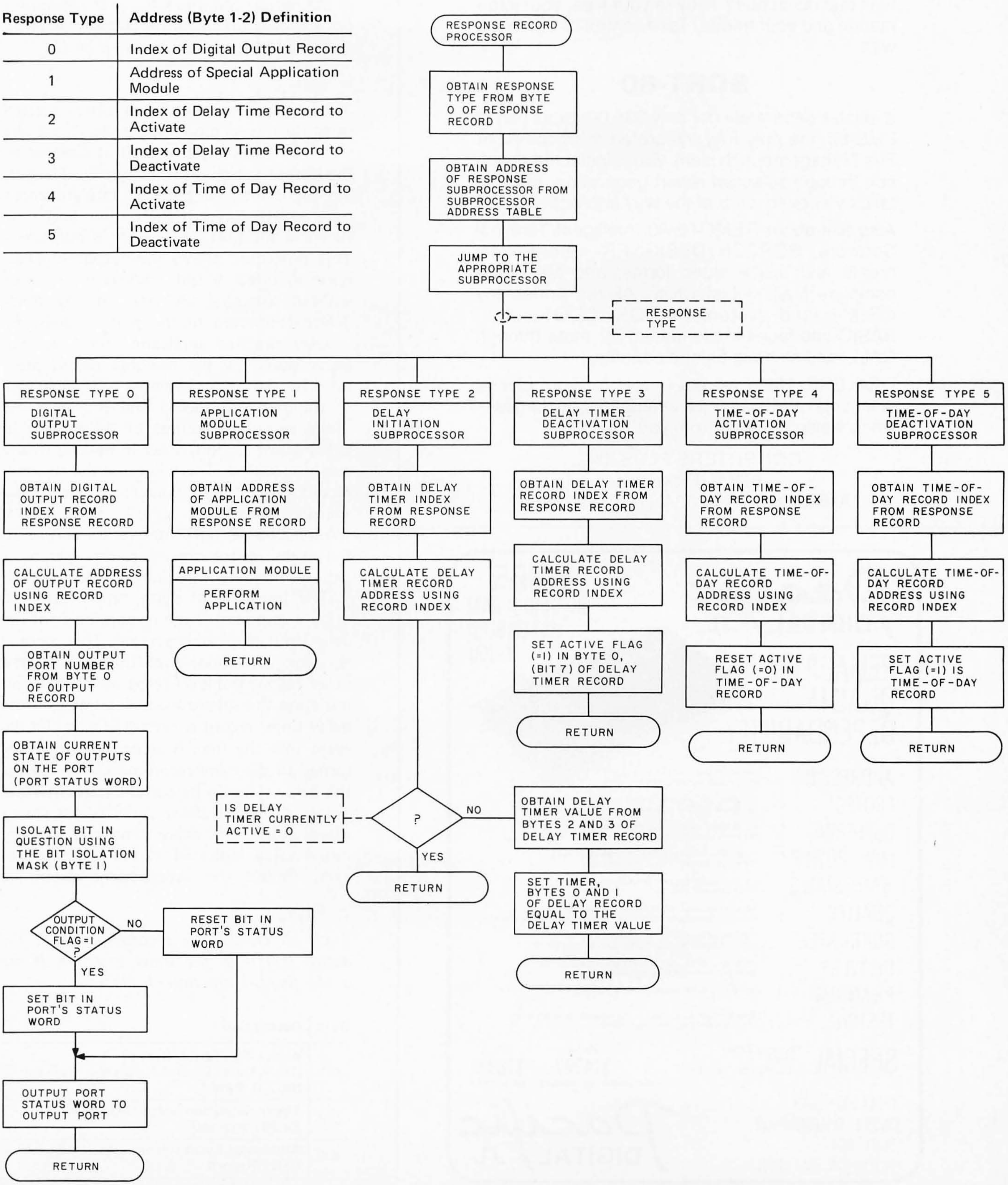
The output port identifier (byte 0) of the digital output record is used to extract the state data from the output port state file.

Table 5: Response record format.

Byte	Description
0	Type of response to be performed (value = 0-5)
1-2	Address of module or record index

Response Type	Address (Byte 1-2) Definition
0	Index of Digital Output Record
1	Address of Special Application Module
2	Index of Delay Time Record to Activate
3	Index of Delay Time Record to Deactivate
4	Index of Time of Day Record to Activate
5	Index of Time of Day Record to Deactivate

Figure 9: Response record processor logic diagram.



Byte	Description
0	Output Port for Output
1	Bit Isolation Mask
2	Output Condition Flag

Table 6: Digital output record format. If the output condition flag is 0, the output bit is turned off (0). If the output condition flag is 1, the output bit is turned on (1).

The bit to be operated upon is then isolated using the bit isolation mask (byte 1), and the state of the bit is set or reset as directed by the output condition flag (byte 3). The output bit is then merged back into the port's state word, stored in the output port state file, and the port's new state is outputted. This procedure allows the output subprocessor to effect a state change on a device without affecting the state of any other device connected to the port in question.

User supplied application modules may be activated by the response record processor by setting the response type equal to 1 in the response record and providing the initial execution address of the module in bytes 1 and 2 (low order in byte 1) of the response record. This will cause the response record processor to execute a jump to the specified execution address. Since all response subprocessors must return control to the event record processor, the user must exit his module with a return instruction.

The initiation of delay timers (used to delay a response) is the responsibility of the delay initiation subprocessor. This module is, upon activation, given the index of the delay record (table 7) to be initiated. Upon initiation the subprocessor determines if the delay timer record is currently active. In the event that the time is active, control is returned to the event record processor, leaving the delay timer in its current state. In other words, an active delay timer is not reactivated, nor is its delay time reset to the initial value indicated in the record. However, should the subprocessor determine

Table 7: Delay time record format. If the active flag is 0, the timer is active. If the active flag is 1, the timer is inactive.

Byte	Description
0-1	Active Flag (Bit 7, Byte 0) Delay Time (Seconds)—(Bit 6-0, Byte 0, Bit 7-0, Byte 1)
2-3	Timer Activation Value (Maximum value = 32,767 seconds)
4-5	Address of Event Record associated with Delay Record

Byte	Description
0	Active Flag (Bit 7) Hours (Bit 6-0) (0-23 hours)
1	Minutes (0-59 minutes)
2-3	Address of Event Record Associated with Time of Day Record

Table 8: Time of day record format. If the active flag is 0, the record is active. If the active flag is 1, the record is inactive.

that the record is inactive, the active flag is reset, the timer's activation time is transferred to bytes 0 and 1 of the record, and control returns to the event record processor.

The deactivation or disabling of active delay timers is the responsibility of the delay timer deactivation subprocessor. This module is passed the index of the delay time record to be deactivated. Using this data the address of the record in question is determined and the active flag (bit 7, byte 0) is set equal to 1, thereby disabling the timer. This same procedure is also used to deactivate a time of day record (table 8).

The activation of a time of day record is performed by the time of day activation subprocessor. This module is, upon activation, given the index of the time of day record (table 8) to be initiated. Upon initiation the subprocessor will determine the address of the record and the active flag (bit 7, byte 0) will be reset (0), thereby enabling the time of day record. The subprocessor will then return control to the event record processor.

Timer Processor

As stated in part 1 (January 1979 BYTE, page 56), a real time clock with a frequency of 1 Hz was used to provide the time base for the system. This periodic signal causes the processor to generate an interrupt, thereby causing the current contents of the program counter register to be saved on the stack and control to be given to the timer processor (figure 8). The functions of the timer processor are:

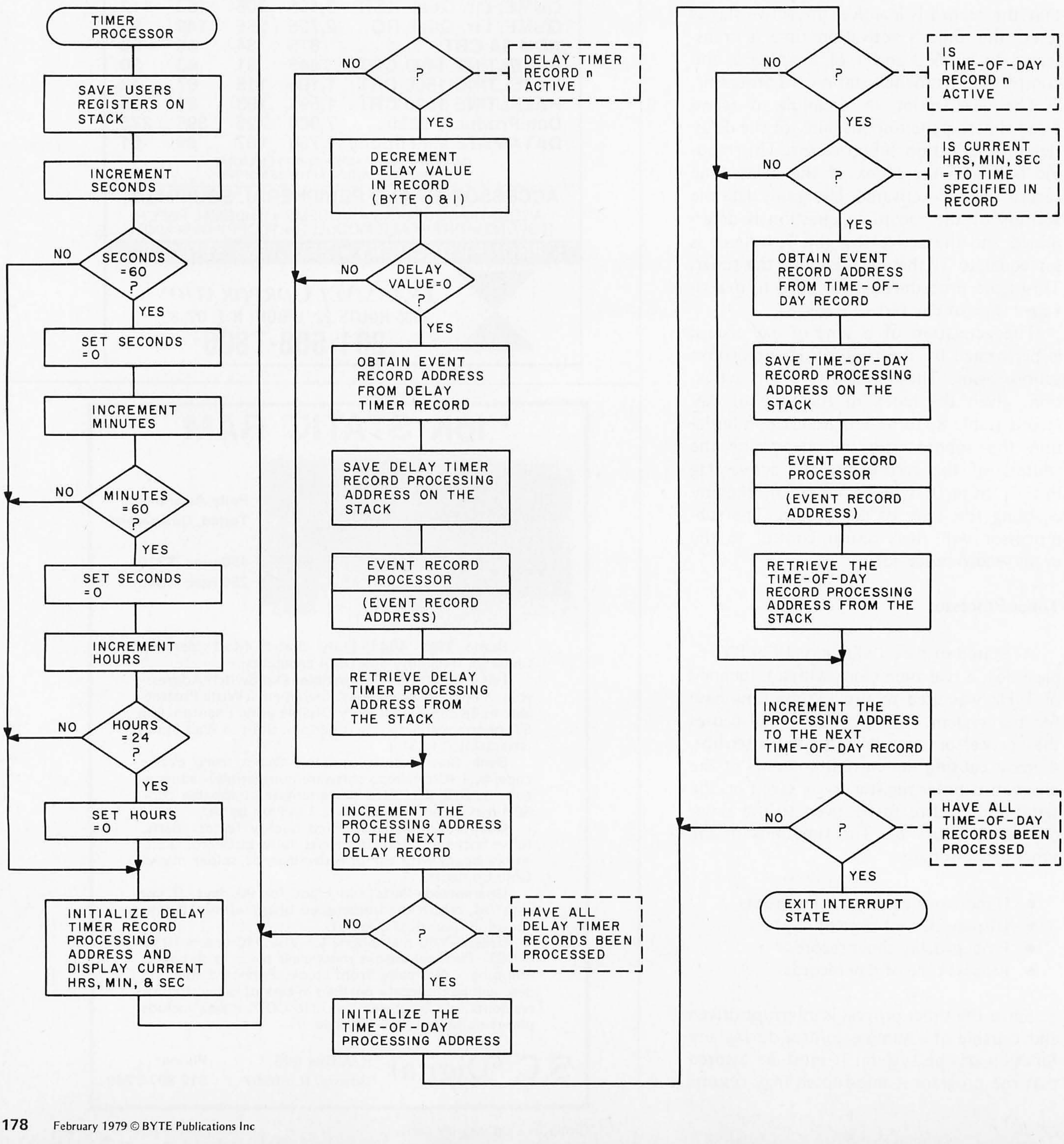
- Handle real time clock interrupts
- Display current time of day
- Process delay timer records
- Process time of day records

Since the timer process is interrupt driven and capable of assuming control during any function of the system, it must be assured that the program it interrupted may resume

execution. To assure this capability, the timer processor immediately upon activation saves the registers of the interrupted program on the stack. Using this technique it is possible upon completion of the timer processor to restore the registers to the state they were before the interrupt and to return control to the interrupted module.

Upon completion of the saving of the interrupted modules registers, the time of day being maintained by the computer is updated and displayed. Hours are displayed in the upper two digits of the address display, minutes in the lower two digits of the address display, and seconds in the data display. To avoid any ambiguity in discerning AM from PM, time is maintained using a 24 hour clock. In this system, then, 0 hours, 1 minute, 0 seconds corresponds to 12:01 AM; 13 hours, 0 minutes, 0 seconds corresponds to 1 PM.

Figure 10: Timer processor logic diagram.



The timer processor scans the file of delay timer records (table 7) to process those records which are active. The function of the delay timer record is to provide a delay of a preset number of seconds before processing an event record. To demonstrate how this function works, let's assume that one wishes to activate an audible alarm 50 seconds after a particular sensor has been tripped. You would structure the event and response records so that the tripping of the sensor would activate the delay timer record you were associating with this event. The activation of the delay timer causes the active flag to be reset and the timer activation value (bytes 2 and 3) to be transferred to the delay time. In our example this will cause the value 50 to be loaded into bytes 0 and 1 of our delay timer value.

As each real time clock interrupt causes the timer processor to scan the file of delay time records, it will find that our record is active. Once the processor determines that a record is active it will decrement the current delay time remaining and then check to see if the time remaining is zero. If there is still delay time remaining (time greater than zero) no further action is taken.

However, if there is no time remaining (time equals zero) the active flag is set, the current registers saved, the address of the event record is extracted from the delay time record, and control transferred to the event processor. The sequence of operations performed from this point will directly result in the audible alarm being turned on.

The processing of the records in the time of day file (see table 6 for record format) is performed upon the completion of all delay time records. Time of day records are processed in a manner very similar to that described for delay timer records. When an active record is encountered during the scan of the time of day file, the current time of day being maintained by the system will be compared to the time of day specified in bytes 0 and 1 of the record. Should these times be identical, the records flag is set to 1 and the processing of the event record specified in bytes 2 and 3 is initiated as described above. After servicing all records in the time of day file, control is returned to the interrupted modules.■

Next Month: *Part 3 of the Computerized Security System illustrates the design of some of the sensors, gives listings of a few of the control modules, and describes the design of the remote sensor display panel.*

Hamming Error Correcting Code

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One of the most frustrating aspects of computers is that they make errors. Large computers have ample redundancy and error correcting hardware to make these errors virtually nonexistent, but owners of smaller computers must typically live with the problem. These errors are not all due to unreliable hardware; they are also caused by noisy environments, line crosstalk, power fluctuations, thermal variations and so on. To meet these problems several techniques have been developed. One of them is called Hamming codes.

The use of Hamming codes is analogous to the use of the common parity bit. A single parity bit merely provides detection of single bit errors, however. In contrast, the Hamming code described herein corrects single bit errors and detects double bit errors. An ideal use for Hamming codes is in cassette recording where single bit dropouts due to tape inconsistencies are common. Larger computers also use Hamming codes to detect and correct memory errors.

Alas, as with all real systems, you don't get something for nothing. To record eight bits of data without any error detection or correction scheme requires only eight bits of memory space. To use the common parity bit approach adds only one more bit of data: nine bits of memory space. But the Hamming code described here requires eight extra bits of memory space for every eight bits of data recorded. There are other Hamming codes available which use considerably less extra memory space per data space, but this one is particularly appropriate for microcomputers and for cassette recording, the most frequent source of errors in a typical hobbyist microcomputer system.

No attempt will be made to discuss the mathematics behind Hamming codes. The reader is referred to any good book on data transmission or error correcting codes for more information.

Building the Hamming Code

Building the Hamming code information is as simple as a table lookup. Every byte (eight bits) of data is recorded a nybble (four bits) at a time. Also, each group of four bits of data has four bits of Hamming data appended so that each byte of data to be recorded actually requires two bytes of storage.

Recording a byte of data is straightforward. Take the leftmost (most significant) nybble of data and record the corresponding byte of data shown in table 1. Next take the rightmost or least significant nybble of data and, again, record instead the corresponding byte from table 1.

For example, to record the data byte, hexadecimal 1F, perform the following:

- Extract the leftmost nybble (hexadecimal 01).
- Replace with corresponding byte from table 1 (hexadecimal E1).
- Record the byte.
- Extract rightmost nybble (hexadecimal 0F)
- Replace with corresponding byte from table 1 (hexadecimal FF).
- Record the byte.

Thus the single hexadecimal byte 1F is actually recorded as the two hexadecimal bytes E1FF. If it is not already obvious, each byte in table 1 has the actual data in its rightmost nybble and error correcting data in its leftmost nybble.

Reconstructing the Data

We are now ready to see how the Hamming code functions. As each byte of stored data is retrieved, with or without errors, four parity bits are constructed which give information as to the correctness of the retrieved byte. Using these parity bits, any required corrections are made to the re-

Data Nybble	Hamming Byte
0	00
1	E1
2	72
3	93
4	B4
5	55
6	C6
7	27
8	D8
9	39
A	AA
B	4B
C	6C
D	8D
E	1E
F	FF

Table 1: Table for transforming data nybbles into Hamming code bytes for storage.

trieved byte after which the original nybble of data is extracted.

Parity bit 4 (P4), the most significant parity bit, is simply the parity of the entire 8 bit retrieved byte. If the 8 bit data word has an odd number of 1s, then P4 is set to 1. Similarly, if the 8 bit data word has an even number of 1s, P4 is set to 0. To form parity bit 3 (P3), the 8 bit data word is first ANDed with hexadecimal 27 and the 8 bit parity of the result determines P3 just as P4 was calculated. Likewise parity bit 2 (P2) is formed by ANDing the retrieved data word with hexadecimal 4B; parity bit 1 (P1), the least significant parity bit, is formed from ANDing the retrieved data word with hexadecimal 8D. Table 2 shows a sample calculation of the parity bits when hexadecimal is retrieved.

Error detection and correction is performed by detecting one of three cases:

- If all four parity bits are 0, the retrieved data word is correct. The original nybble of data is correctly formed in the rightmost nybble of the retrieved data word.
- If P4 is 0 but one or more of the parity bits P1, P2, or P3 is not 0, then a double bit error has occurred. The program should probably inform the operator and then halt.
- If P4 is not 0, a single bit error has occurred, which can be corrected.

To correct single bit errors, a byte chosen from table 3 is exclusive-ORed with the retrieved data byte. Parity bits P3, P2, and P1 (P3 is most significant and P1 is least significant) determine which byte to select from table 3. Table 4 demonstrates the correction and detection process for several different cases.

Data Word	AND	Result	Parity Bit
01100111	—	01100111	P4 = 1
01100111	00100111	00100111	P3 = 0
01100111	01001011	01000011	P2 = 1
01101111	10001101	00000101	P1 = 0

Table 2: A sample calculation of parity bits for the binary data word 01100111 (hexadecimal 67). Since P4 is not 0, a single bit error has occurred, which can be detected (see text).

P3	P2	P1	Error Correction Byte
0	0	0	10
0	0	1	80
0	1	0	40
0	1	1	08
1	0	0	20
1	0	1	04
1	1	0	02
1	1	1	01

Table 3: Single bit error correction table.

Case 1: No errors.

Data	AND	Parity	Comments
E1	—	P4 = 0	All parity bits 0 implies no error.
E1	27	P3 = 0	
E1	4B	P2 = 0	
E1	8D	P1 = 0	

Case 2: Single bit error.

Data	AND	Parity	Comments
E3	—	P4 = 1	P4 not 0 implies single bit correctable error.
E3	27	P3 = 1	P3P2P1 = 110
E3	4B	P2 = 1	Corrector from table 3 = 02
E3	8D	P1 = 0	Data E3 Exclusive OR 02 Correct data E1

Case 3: Single bit error.

Data	AND	Parity	Comments
C1	—	P4 = 1	P4 not 0 implies single bit correctable error.
C1	27	P3 = 1	P3P2P1 = 100
C1	4B	P2 = 0	Corrector from table 3 = 20
C1	8D	P1 = 0	Data C1 Exclusive OR 20 Correct data E1

Case 4: Double bit error.

Data	AND	Parity	Comments
E2	—	P4 = 0	P4 equal to 0 and P3, P2, or P1 not 0 implies a double bit error.
E2	27	P3 = 0	Note: data in P3, P2, and P1 for a double bit error does not imply any information about which bits are in error.
E2	4B	P2 = 0	
E2	8D	P1 = 1	

Table 4: Examples of uses of the Hamming code. For each case the transmitted information is hexadecimal E1. When a 1 bit error is detected, the parity bits P3, P2, and P1 are used to look up a correcting factor from table 3.

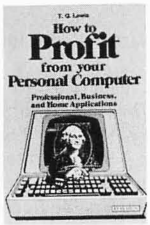
Conclusion

The algorithm described here has been programmed on several different microcomputers. Not many bytes of program are actually needed and the benefits are great. One need only read a large program from tape into main memory several times to realize the utility of the approach. If your current read in software informs you of any errors encountered, you probably must still find the errors and correct them, assuming you even know what the correct data should be.

Hamming codes can be extended to correct double bit errors, or to perform any practical *n* bit detection and *m* bit correction, but the extra memory costs can climb fast. Also it is very easy to build a hardware Hamming generator and detector using only a few discrete integrated circuits.

The Hamming code described here is both practical and valuable. Manufacturers should seriously consider incorporating this technique in hardware. The cassette enthusiast should incorporate this technique in any standardization or interchange effort. Even the everyday experimenter will find that the hour spent programming the algorithm will save many hours of frustration in the future.■

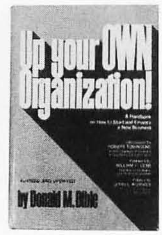
Get Down to Business



How to Profit From your Personal Computer

by Ted G Lewis

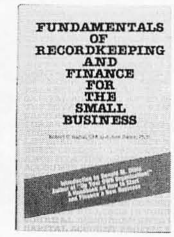
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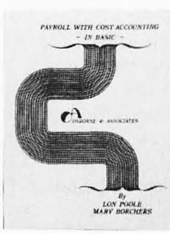
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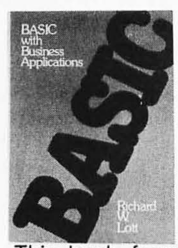
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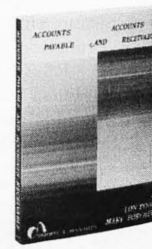
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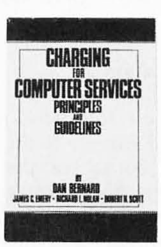
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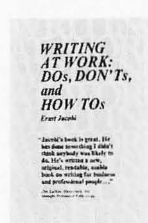
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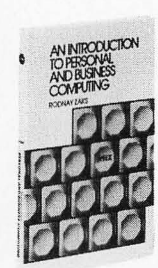


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The TRS-80 Club of Arlington MA is offering a free semiannual newsletter. For a copy, send a SASE to *TRS-80 Newsletter*, 96 Dothan St, Arlington MA 02174.

User Group for TRS-80 Owners North of San Francisco

A TRS-80 user group has been formed north of San Francisco. Called the Redwood Empire TRS-80 Users Group, it is handy for owners in Sonoma, Marin, Lake, and Mendocino counties. Anyone is welcome regardless of whether or not they own a TRS-80. Contact John Revelle, 7136 Belita Av, Rohnert Park CA 94928.

New Computer Club Formed in Greene County MO

A group of small computer users met in October 1978 for the purpose of organizing a computer club within the greater Greene County MO area. Two user groups were formed and the decision was made that separate users groups would be formed representing computers which have four or more users. The existing user groups are IBM 5110/5100 and Radio Shack TRS-80. The dues are $12 a year, which includes a newsletter. Anyone in the Ozarks area interested in the club or in one of the user groups should contact Andrew Griffin, 2145 W Central Av, Springfield MO 65802, (417) 866-2447.

The Liberated Calculator Users Club

A number of the readers of the newsletter *Calculator Lib* (see "Clubs and Newsletters," January 1978 BYTE, page 141) have organized The Liberated Calculator Users Club, an independent group of calculator users dedicated to exploring the limits of the state of the art in calculator mathematics. Their goal is to profit mutually from members' knowledge of calculators and related fields and create a forum that allows club members to meet and identify with each others' interests. Contact Gene Hegedus, POB 2151, Oxnard CA 93034.

ACG-NJ News

The Amateur Computer Group of New Jersey continues to publish the impressive *ACG-NJ News*. This 20 page monthly publication is packed full of informative articles, club news, interesting tidbits about the computer industry, and much more. Membership to ACG-NJ is $15 a year (US and Canada) and $12 (foreign). Contact ACG-NJ, UCTI, 1776 Raritan Rd, Scotch Plains NJ 07076.

Microware Products Users Group

A users group for Microware products, which include the RT68 multitasking monitor and the ABASIC compiler, has recently been formed. The name of the newsletter is *Microware Forum*. The first issue contains adaptations of the compiler to video terminals, printers and the SwTPC calculator card. A year's subscription is $10. Contact Microware Forum, POB 3630, Minneapolis MN 55403.

New TRS-80 Publication

The *80-Northwest Journal* is a new publication devoted entirely to the TRS-80 computer. The journal features complete BASIC and machine language program listings. It covers the entire spectrum of TRS-80 capability, including programs and articles on business, audiovisual and scientific applications, and games. Currently it is running a series on machine language programming for beginners. Hardware features and product reviews are also included. The *80-Northwest Journal* is published bimonthly by 80-Northwest Publishing, POB 7112, Tacoma WA 98407. The subscription price is $16 per year.

Poly-88 Users Group Expands Services

The Poly-88 Users Group has announced expansion of services to PolyMorphic 8813/8810 disk system owners. Most of the current library of programs for the Poly-88 will be available on a

basis similar to the cassette versions. Members may contribute a new program in exchange for a program from the library or credit for a future choice. Members may also request programs for $2.50 each for handling and shipping on a furnished disk. Optionally, the users group will also provide the blank disk for $3. The membership fee is $5 (US, Canada and Mexico), $15 foreign and includes 12 issues of the newsletter which is published every two or four months depending on the number of additions to the library and general news of interest to Poly owners. Contact Poly-88 Users Group, 1477 Barrington #17, Los Angeles CA 90025.

Atlanta Computer Society

The Atlanta Area Microcomputer Hobbyist Club has changed its name to the Atlanta Computer Society. Meetings are held the last Wednesday of each month at 7:30 PM. The meeting location is the Community Room of Decatur Federal Savings and Loan Association, Dunwoody Branch, 1630 Mount Vernon Rd, Dunwoody GA. Visitors are welcome. For more information, write ACS, POB 88771, Atlanta GA 30338.

Attention: New York City TRS-80 Owners

We have been notified of the existence of a TRS-80 users group in New York City. Called the Metro TRS-80 Users Group, they meet the second Wednesday of every month at the Beverly East Bridge Club, Beverly Hotel (third floor), 125 E 50th St, New York NY. The meeting time is 6 PM and there is a $1 admission fee.

Newsletter for RCA VIP Owners

The VIPER is an independent user newsletter dedicated to the RCA COSMAC VIP. The $15 subscription price includes ten issues of volume 1. The first three issues contain articles revealing the machine language code for CHIP-8 (the VIP's user language), an annotated listing of the operating system and the first in a series of articles describing a text editor for the VIP. Contact *The VIPER*, POB 43, Audubon PA 19407.

Toronto Region Association of Computer Enthusiasts

TRACE is the monthly newsletter of the Toronto Region Association of Computer Enthusiasts (TRACE), POB 545, Streetsville, Ontario CANADA L5M 2C1. Membership in the association is open and dues are $15 per year, which includes the newsletter and admission to all meetings. The newsletter is available separately for $7 per year. The association has two meetings each month; one at the Ontario Science Ctr, 770 Don Mills Rd, Toronto at 2 PM on the second Sunday of the month; and the other at Humber College, Rexdale, at 7:30 PM on the fourth Friday of each month in room J209.■

Mark Klein
Sanborn Regional School District
Kingston NH 03848

A computer's power comes from several sources, including its speed, memory, and the logic capability of its software and hardware. This article is about computer memory — in particular, it describes files, the organizational structures computers use to manage information on secondary memory devices like disks and cassettes. What kinds of information are kept in files, how different devices store files, how programs use files, and how operating systems manipulate files are subjects that will be covered in this 2 part article.

Files on Parade

Part 1: Types of Files

Since the subjects apply to all computer systems and are largely the same from one computer system to another, the material is presented in general terms. In fact, it is the generality of the concept of files and file techniques that makes them so powerful and so much fun to use. But specific examples help us learn, so scattered throughout the article are descriptions of how the concepts are implemented on the three computers I use regularly:

- A microcomputer (TDL Xitan 2, with audio cassette and dual PerSci floppy disk drives, at Sanborn Regional High School.
- A minicomputer (DEC PDP-11/10 with dual digital cassettes and 2.5 megabyte hard disk drive, also at Sanborn Regional).
- A big midicomputer (DECsystem-10 with 1 megaword of main memory and all the trimmings, at the University of New Hampshire).

The microcomputer needs no justification. The minicomputer is interesting because its RT-11 operating system and Multiuser BASIC are the same systems DEC uses for its LSI-11 based PDP-11/V03 with floppy disks. The LSI-11 of course is the heart of the Heathkit H11 system. The DEC-10 is included because its big system features are appearing on the newer microcomputers.

What's in a File?

Anything can be kept in a file. That's reason number one for the importance of files. There are several ways to organize files, and one of the simplest ways is to separate them into program files and data files. Program files could include a BASIC game or business payroll program, a FORTRAN compiler, an assembler, a text editor, a debugging tool — in short, anything from higher level language application programs to system software.

Programs with little data handling often keep the data right in the program (using, for example, the READ and DATA statements in BASIC), but the more powerful and versatile technique is to store the information in data files. In that way several programs can access the same data by calling that data file, or one analysis program can call in several different data files. A simple example of the latter type might be a payroll program that works on the data file containing this week's time clock records today, and next week uses a similar data file containing employee work records for that week. The data in these files could be strings or integers or floating point numbers.

Sometimes the distinction between program files and data files becomes blurred. Using a software tool such as a text editor we could produce the source listing for an assembly language program. In the sense that this listing is an output file from the text editor and is destined to be an input file for another tool, the assembler, it is certainly a data file. However, it is most often called a *source program* because eventually, after we feed it through a few more programs (called linkers, loaders, and debuggers), we do run it as a program. (For a brief but clear description of the functions of these software tools, see "Beyond BASIC" by Alan B Salisbury in November-December 1976 *Creative Computing*, page 28.)

ASCII versus Binary Files

A different way to organize information is by the kind of characters used to encode the information in the file: ASCII or binary. The full ASCII character set includes the digits 0 thru 9; upper and lower case letters; special symbols like parentheses, comma, and semicolon; and control characters like carriage return, record separator(RS), end of

file(EOF), and start of header(SOH). Binary encoding means that only logical 1s and 0s are used. Executable object programs are commonly kept in binary files.

When a software supplier wants to keep the inner workings of one of its products a secret, that piece of software is supplied as an object program, typically in binary. A listing of the sources in some higher language is often available but at additional cost. Thus our Multiuser BASIC from DEC was delivered as a binary file. For other binary files in our systems, we might also have the source listings in ASCII files. In this category are FORTRAN or assembly language programs that were fed into assemblers or compilers to produce the binary files. Both programs and data can be encoded in binary files, as shown in table 1.

Many kinds of programs and data are stored as ASCII files, including text files for word processing programs, BASIC application programs, assembly source files, and mailing lists. ASCII files often use only a subset of the characters in the full 128 character set. Common subsets are the 64 character set with only upper case characters, the Radix 50 set, and the ASCII hexadecimal set (0,1,...,9,A,B,...,F), among others. The floppy disk handler program on our microcomputer for example is stored in ASCII hexadecimal format. Listing 1, produced with the TDL Zapple monitor's S command, shows the part of this file which was loaded into memory beginning at hexadecimal F900.

Types of File Access

As we have seen, there are many ways to characterize files. The most illuminating way, and for the programmer the most important way, is in terms of how a file is accessed, either sequentially or randomly. A typical file is composed of header or label, data items, and an end of file mark. These components are contained in subdivisions of the file called records or blocks. (See "Fundamentals of Sequential File Processing," October 1977 BYTE, page 114, for a full description of one kind of sequential file.)

```
 sF900 DB- C1- 2F- E6- C0- C2- 13- F9-
F908 CD- AE- F9- CD- 70- F9- 3E- 04-
F910 CD- 8E- F9- CD- 7A- F9- DA- 1F-
F918 F9- CD- 49- FA- C3- 13- F9- FE-
F920 04- CA- 7C- F0- FE- 01- CA- 31-
F928 F9- FE- 05- CA- 4E- F9- C3- 13-
F930 F9- 2A- AA- F9- CD- 09- FA- CD-
F938 7A- F9- DA- 42- F9- 77- 23- C3-
F940 37- F9- F5- 2B- 22- AC- F9- CD-
F948 09-
```

Listing 1: ASCII hexadecimal format file generated by using the TDL Zapple monitor.

The best way to access a file depends on whether the whole file or just part of it is needed. When loading a higher level language application program from disk into memory the whole file is required in memory in serial order. But when updating an item in a data base, one usually wants to address one or two bytes within a record. Between these two extremes are applications in which a program calls one or more records from a file, such as an assembler processing a source file, reading a statement at a time from the input file. Each of these applications has an access type, sequential or random, for which is it best suited.

Advantages of Random Access

Before choosing an access type for a file, one should understand the difference between them, as summarized in table 2. The first two rows point out a major difference:

Table 1: Examples of information types used in files.

File Used As \ Character Type	ASCII	Binary
Program	assembly language source listing BASIC application program	the Multiuser BASIC interpreter object modules from assembler
Data	mailing list	virtual arrays

Table 2: Comparison of sequential versus random access files.

File Characteristic \ File Type	Sequential	Random
file contents accessible in sequential order	yes	yes
file contents accessible in random order	no	yes
speed of access to a particular record	slower	faster
file size	variable — can change with each update	usually fixed at time of creation
method of creation	under application program control, *or* using a text editor	usually under application program control
method of update	must rewrite the whole file	individual elements can be changed
amount of data transferable as a unit	byte, record, sector *or* file	byte or sector

to get to an item in a sequential file, the user must first read all the preceding items (records, sectors, blocks, or bytes). In a random access file, individual bytes can be directly addressed because information within the file is usually segmented or delimited by a number of bytes. A sequential file might use record separators or end of file marks as delimiters, with a correspondingly larger lower limit on the size of the smallest amount of information transferred.

The same applies when a file is updated. The entire sequential file must be rewritten to change one byte, while individual items can be changed in a random access file without rewriting the whole file. These differences account for the faster speed of access to any given byte in a random access file, since the preceding bytes do not have to be read first. The last byte in such a file can be read just as quickly as the first.

These distinctions make clear why random access files are chosen for data base applications. However, when moving a whole file at once (for example, saving an application program that currently is in main memory on disk), these differences disappear because the transfer is done sequentially as a continuous stream of data bytes. This type of transfer is commonly called *stream IO*.

Virtual Arrays

The shorter access times of random access files are utilized on some systems (for example, DEC's RT-11 and Multiuser BASIC) to provide a virtual array facility. Instead of moving a data structure into primary memory and then operating on it, the data structure is stored in a random access file. Whenever the user's program wants to operate on a piece of the data, the system fetches that piece from the file, letting the user pretend that the piece of data is already in primary memory. The jargon phrase for "letting the user pretend" is "making the data fetch transparent" to the user.

The reason for having virtual array capability is that application programs can use virtual arrays to handle data structures too large to fit into primary memory. Large arrays can be stored on the disk, with only a portion of the file in primary memory at one time. Since virtual arrays (containing string or numerical data) are usually stored as unformatted binary data, IO conversions can be eliminated during storage and retrieval. This means no loss of precision, nor time wasted doing conversions.

The most visible difference between a real array and a virtual array is the time needed to access a particular array element as a function of where that element is in the array (its referencing order). For real arrays, access time is independent of referencing order; for very large virtual arrays, referencing order could noticeably affect program execution time. Knowing the algorithm used by the virtual array processor to search the random access files can help optimize the user's program, but any execution time differences are a small price to pay for the ability to handle the data in the first place.

Sequential Access

All the advantages do not lie with random access files. The need to update the whole sequential file at update time carries it with some built-in flexibility. The size of the file can expand or contract to match the size of the file contents. Random access file size is usually fixed at the time of creation. If the random access file is used to handle, say, a data base, a guess must be made at creation time as to the maximum number of items in the data base. If the guess is far too big, a lot of the storage device where the file resides may be tied up unnecessarily, with large blocks reserved for data that never appears. If the guess is too small and data threatens to overflow the fixed file space allocated to it, a programmer will have to create a new file, with larger file size parameters, and then transfer the data from the old file to the new one. Foresight and good system design can avoid both extremes, but it is easier said than done.

Sequential files can also be more convenient to create, since there are often more ways to do so than for random access files. For example, data is usually entered into a random access data base under the control of an application program. This program calls for the data at some input port and transfers it to the file. The flexibility of this process and the opportunity for error correction and verification depend on the flexibility of the application program.

This same method is also used for sequential files, but there are other ways, too. Several kinds of sequential files, both program and data, can be created using the system's text editor with its generally powerful editing capability. In some cases, for instance in the DECsystem 10's BASIC, some sequential files are directly listable at the user's terminal without having to write a program that calls the file into main memory and then prints it out piece by piece. These directly listable sequential files can then be edited easily using commands that delete or change lines.

The capability for direct listing is related to how the information is stored. Binary characters, used for virtual arrays, are usu-



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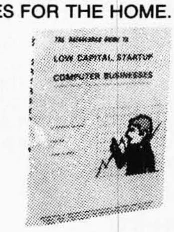
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ally transmitted through a parallel IO port interface such as might connect a floppy disk unit to the processor board. However, most terminals are connected by a serial interface and handle ASCII characters.

Input and Output Modes

Another file characteristic that sorts according to file access type is the need for file mode, either input (read) mode or output (write) mode. When a program needs to access a sequential file, that file must first be placed in the appropriate mode. Setting or resetting the mode moves the data pointer to the beginning of the file so that the access can be sequential from the start of the file.

Access Method	Storage and Retrieval	Delimiter	Access Type
Stream	as a continuous stream of data bytes	next file name	sequential
Punctuated	as a sequence of variable length records	ASCII RS character	sequential
Relative	as byte addressable random access memory	number of bytes	random or sequential
Direct	as specific sectors on specific tracks	sector number	random or sequential

Table 3: Various file access methods used by the PerSci floppy disk operating system.

(a)

```
 k
*Q*/1
FILES 08-09 09 771219
TEXTPROC.TDL        01-01 0023 0022 064 771219 771219
BIGRUMP.TDL         01-24 0074 0073 033 771219 771219
BASIC.TDL           04-20 0065 0064 001 771219 771219
EDIT.tdl            07-07 0023 0022 001 771219 771219
IODRIVER.EEN        08-04 0005 0004 051 771219 771219
```

(b)

```
 ^C

.R PIP
**.MPK/L/C/W
19-DEC-77
TESFIL.MPK     1 19-DEC-77   7321
TALK2 .MPK     7 19-DEC-77   7322
LEVEL2.MPK     5 19-DEC-77   7331
FILART.MPK    12 19-DEC-77   7336
4 FILES, 25 BLOCKS
1323 FREE BLOCKS
*
```

(c)

```
DIRECT

DSKC:    [2000,10146]
PBOOT    STC    10  <057>   23-Nov-77
HART     APL    12  <057>   26-Jul-77
SWITCH   INI     1  <055>   13-Nov-77
PFAM     TXT    14  <057>   17-Nov-77
EEN      APL    39  <055>   19-Jul-77
HARTLO   ADA    49  <255>   27-Jul-77
  Total of 125 blocks in 6 files on DSKC: [2000,10146]
```

Table 4: Three tables showing the displayed file organization on three different processors. Table 4a is a TDL Zapple microcomputer floppy disk directory. Table 4b shows a disk directory from a PDP-11. Table 4c is the user's directory from a DECsystem-10.

Usually random access files do not distinguish between input and output mode; a data pointer is merely set to the point of access. In practice, the necessity to set the mode for sequential files is only a minor inconvenience.

Other differences between sequential and random access files may exist under particular languages or operating systems. These differences can be very important locally as software producers add extensions to standard languages to gain a competitive edge (see table 3 for one manufacturer's file management system). The programmer's job is still to choose the file access category that best fits the program being designed.

Devices That Hold Files

A computer system is a collection of devices, many of them addressable: disks, magnetic tape drives, cassettes, card or paper tape readers, paper tape punch, printers, terminals, etc. Files can be transferred to and from all of these devices, but of the devices mentioned, only disks are random access devices — devices that allow data to be processed in random order independent of its physical location on the device or its location relative to other information. These devices are sometimes called *block replaceable* devices. The other devices process information in the same order as the physical order of the data on the device. These are called *sequential access* devices.

File Structured Devices

Disks, tapes, and cassettes are all file structured devices; ones that allow the storage of data under assigned file names. In some systems that use audio rather than digital cassettes, this could be a minimal storage system. The TDL 8 K BASIC, for example, lets the user store files with a 1 letter file name on cassette. Reading that file requires proper manual positioning of the tape, but since it won't load back into memory unless the load command addresses the file by its correct 1 letter title, it is probably legitimate to call those cassettes file structured. Devices which are not file structured contain a single logical collection of data, such as a line printer or terminal.

Directory Devices

The file structured devices can be further classified according to whether or not they are directory devices. A directory device is one that contains a table of contents with critical information about the files on that device. Tables 4a, 4b, and 4c are partial

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Device	Access Type	Directory?
disks	random	yes
magnetic tapes	sequential	varies with operating system
cassettes	sequential	no

Table 5: Comparison of three file structured devices in order of increasing access time.

file directories from various processors. Besides the file name and date of creation or modification, the directory contains the size and address of the file on the device, although the directory listing on the terminal may not show all of this information. File access times are orders of magnitude faster on directory devices because the hardware can first examine the directory and then go right to the sector where the wanted information resides.

Table 5 summarizes the access time comparison for file structured devices and shows why cassettes are so much slower than disks: they are neither random access nor directory devices. Even a digital cassette drive run by an intelligent controller must spin a lot of tape, examining each file header in turn until it finds the one desired. To appreciate the time differences involved, consider the time it takes to load the TDL 8 K BASIC interpreter on our microcomputer: using the fast TDL cassette format (1200 bps), the cassette tape takes 3.5 minutes; and using the PerSci floppy disk, it takes about 2 seconds.

Magnetic tapes occupy the middle ground between cassettes and disks because while they are sequential, they can have high data transfer rates. But as with cassettes, updated files must be tagged onto the end of the tape, drastically increasing their access time. Cassettes and magnetic tapes typically contain directory type information headers at the beginning of each file, so the system can at least read them sequentially and produce a table of contents on the user's terminal. Magnetic tape units, however, are seldom seen on microcomputer systems because they are much more expensive than floppy disks.

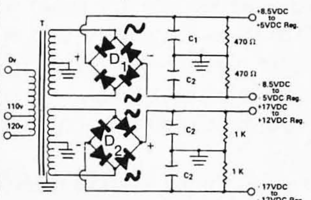
Today, floppy disks represent a good trade-off between price and performance (speed and information capacity) in handling files. But remember that files are just a way of organizing memory, and newer memory devices like bubble memories and charge coupled devices are likely to change people's opinions about the best ways to handle files.

Part 2 of this article will describe the detailed techniques of managing files.■

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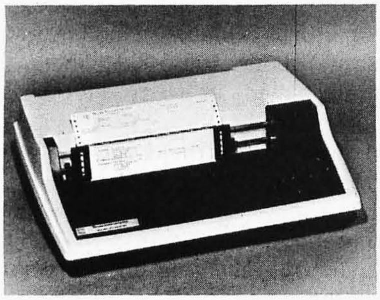
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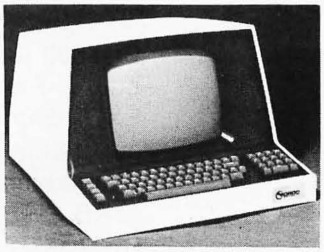


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Continued from page 7

Raphael's book *The Thinking Machine: Mind Inside Matter,* required a Xerox XDS-940 computer with 64 K 24 bit words of memory in its first version circa 1969. In the second version of Shakey, the robot was driven by a PDP-10 with roughly 200,000 words of 36 bit memory (ie: close to a million bytes of memory.) Shakey is no doubt one of the best mobile robotic systems seen to date.

The advances in computer power allow many more individuals to experiment with such mechanisms. The present crop of microprocessors have a 23 and 24 bit byte address space that is complemented by the extremely large 64 K bit (and in years to come, 256 K bit) dynamic memory parts. These are the latest examples of how microelectronics creates the kind of computer power needed to control autonomous mechanisms inexpensively and, therefore, practically. We are now seeing the possibility of inexpensive (under $1000) computer electronics equivalent to Shakey's 1971 era PDP-10. The processing power needed to make a robot perform complicated visual recognition and manipulation tasks will be available to the creative individual experimenter. Even without the latest state of the art of integrated circuit design, the typical personal computer's 8 bit processor with 64 K address space, floppy disks and displays is more than adequate for experimenting with automated mechanisms including arms and mobile robot platforms.

In this issue we have two articles by various personal computer experimenters on designs of robotic arms that can be built and programmed using readily available components. In the pursuit of the successful robotic system, the arm is one of the most challenging subsystems to design; we are mapping a physical space, getting sensor feedback about the objects in that physical space, and manipulating the objects. Of course, the open loop manipulation of objects without feedback is possible, and is a step in the right direction. But real adaptive interaction with the design evironment requires some form of feedback. Put all these details together, and a challenging project results. It includes elements of software design of the control programs for the system, elements of mechanical design for the proper fabrication of a balanced and reliable arm, and elements of electronic design for the interface between mechanism and logic levels.

The task of designing an arm subsystem as described in this issue's articles has been one of creating it from scratch. But what about the prospect of taking a shortcut by

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purchasing some form of "experimenter's arm" kit?

There has been one attempt at a commercial kit product for the robot arm experimenter, a product which was advertised in this magazine starting last spring. I refer to the Gallaher Research "Grivet" arm, which is shown in photo 1.

The photograph was taken using the kit I bought for $400 and put together one Sunday morning in September. In a phone conversation with Mr Gallaher, I have since been informed that the Grivet will no longer be available by the time this issue reaches readers, although he is filling orders already placed.

Mr Gallaher's robot arm was a crude start at best, for all we got is a rather shaky mechanism with six DC motors. The purchaser's inventiveness must supply the details of electronic interface and control. A suggestion, in the marketing literature supplied with the kit, is that relays be used to provide control of the 6 VDC which will run the motors. This kit provided what you see in the photograph: a limited mechanical start on a complete arm which must include a mounting of some sort, power supplies, bidirectional motor drive electronics, and sensory feedback. There is not even a suggestion of how to mount and use sensors to provide feedback control of the arm in a practical object manipulation environment such as a chessboard with chess pieces as the objects.

The designer of this arm did his homework with respect to balance, for it will sit upright on its counterweight with no particular urge to topple over. The photograph was taken with the arm in this position. But if mounted in a horizontal position as suggested by the sales literature (assembly drawings, but no instruction manual, come with this device) several of the parts are under enough stress to be visibly bent. The only way I can see to practically mount this arm is by having it hang down from the shaft furthest from the hand mechanism (flipping it 180 degrees around the vertical axis of photo 1).

The Gallaher arm kit's parts are apparently handcrafted. When you think of the time and energy that went into its creation, it is obviously a bargain at $400, even if incomplete. Some of the first microcomputer kits such as the Mark-8, Altair and Sphere were similarly incomplete, and a whole industry was formed filling in the gaps to provide a complete computer system in assembled form. Therefore, we can expect more complete robotic systems as further products are offered to the experimenter. Just as "hardheaded realists" (ie: unimaginative people) scoffed only four years ago at the idea of a personal computer, I can almost hear the equivalent comments about domestic robots being uttered as I pen these words at the keyboard of my personal computer.

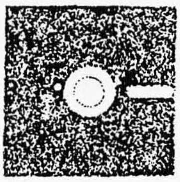
As this text is prepared on November 11 using the editor facilities of the UCSD Pascal system running on a Northwest Microcomputer Systems 85/P, I know of no kit products which are available to the experimenter for creation of the integrated mechanical and electronic parts of an arm such as those described in the articles by Andrew Filo, Keith Baxter and Timothy Daly in this issue. In order experiment with arms, readers will have to use the philosophy of "do it yourself" to create the mechanical

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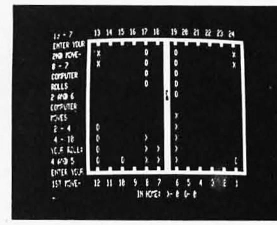
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Circle 327 on inquiry card.

and electrical control parts of the system. This is a philosophy which many people (including myself) have successfully used in learning about and creating homebrew computers from scratch using microprocessor and TTL integrated circuit components. Until we see some commercial products it will be the only way.

Of course, the comments above regarding a paucity of kits apply only to arm mechanisms. There is the Terrapin Inc "Turtle" kit which has been available since this past summer. This mechanism is a product of a group of free spirited indivduals associated with the MIT artificial intelligence laboratory. It is a direct outgrowth of the Logo project which began several years ago. The kit gives one a mobile object mounted on two wheels and casters, but tethered to the computer by an umbilical cord. (The people at Terrapin say a remote controlled version using a sonic system and on board batteries may be in the works for a next model.)

The Turtle, is, of course, intended to be used to teach children (large and small) concepts that are illustrated by motion of a real object which may deposit tracks below it. The Turtle is the ideal real object for demonstrating strategies of search and motion which are a subset of the techniques needed to implement a real version of an "R2D2" robot.

For delighting family and friends with a mobile mechanism, there is an area of peripheral devices which has yet to be discussed in these pages. This is an area which has a fairly obvious and relatively inexpensive open loop output. The kind of device I refer to is the traditional marionette hooked up to computer controlled actuators.

Photo 2 shows an example of a marionette which I purchased with the idea of making this point through a photograph. The marionette cost $32.50 at a wonderful store called Geppetto's located in a pushcart in Boston's Faneuil Hall marketplace. Looking around for actuators, I found a box of tiny DC motors in Eli Hefron's store in Cambridge MA which set me back about $20 for more than enough motors to pull all the strings of this puppet. Counting the electronics and tiny gear boxes needed to pull the strings in a simple binary manner (up or down for any given string) the guts of the marionette output device will probably run less than $75. Add some wood to build a little theater, and the cost of the completed output device will probably total under $100 in parts. Of course, I have not built such a device, and may never get around to doing so. I present the idea as a possibility for some reader to use as a source of some challenging fun.

Control of such a marionette output device can be accomplished with a computer as simple as a single board machine language oriented development kit, or it can be made quite elaborate using the software tools of the more complete personal computers now on the market. The goal of the software support for the marionette is of course identical to the goal of software support for stored performances on a music synthesizer: creation and execution of strings of commands to be sent to the mechanism. The programming of such a project can be handled by the implementation of a special purpose interpretive language using whatever software tools are available.

This brings the discussion back to that all

important question: "How does the personal computer fit into this concept of robotics and the control of mechanisms?" It fits elegantly, due to the software tools that are now so inexpensively available, built into a black box that is the personal computer. To date the tools have been almost exclusively assembly language or BASIC on the bigger machines, and BASIC built into read only memories of the smaller machines. But the boundary line between "big machine" and "affordable by the individual experimenter" is eroding away with the prices of computers. With one appliance computer presently on the market sporting a pseudo-APL as its consumer oriented command language, and Pascal available on the more expensive ($2000 and up) personal computers, can it be long before we see a LISP, small talk, or Logo kernel appearing in the personalities of small computers?

Even if one is confined to BASIC as the built-in personality of a small computer, it is possible to do significant things. I have seen an attempted implementation of LISP, sent in by a reader, using only Microsoft's widely available interpreter (the Applesoft version). Ray Cote of BYTE has also quite effectively adapted and extended a Microsoft BASIC implementation of the macrolanguage called GPM, adding a few features that address the color graphics hardware of the Apple computer. The particular 50 line BASIC implementation he started from was written one weekend last spring by Walter Banks of the University of Waterloo. Each of these examples used the built-in tools of the BASIC oriented computer at hand to build better tools that would prove most useful in the artificial intelligence programs required for robotics experimentation. The GPM interpreter superimposed on the Microsoft BASIC interpreter runs surprisingly fast. Two layers of interpretation isolating the application from the machine language of the 6502 in the Apple do not get in the way of serious experimentation using GPM. I expect that the same will prove true when the LISP interpreter written in Microsoft BASIC is finally debugged in its Applesoft incarnation.

Whatever the kernel of software tools that one has available in the personal computer, one of the most important design considerations is using these tools to create an interpretive language which fits the mechanism. Special purpose interpretive languages are not hard to implement, as I have demonstrated for myself recently, using a 6800 macroassembler to implement an interpretive language for musical texts, coordinating the organ keyboard and music synthesizer peripherals of my homebrew system. Having tools such as my present Pascal system, a LISP or a GPM would certainly have helped this process. But the program had already been nearly completed using last year's tools of my system.

The subject of special purpose interpretive languages for particular applications such as robotics (or music, or household control, etc) is one which is worthy of much tutorial discussion. The problems of designing such a language include identifying the primitive operations required, picking a strategy for creating and debugging interpretive texts, and choosing control structures appropriate for the application. Choosing an existing interpreter for a language such as LISP or GPM as a basis upon

which to build more detailed software is often a good strategy. One can also use the "reinvent the wheel" method at a low level, as I did with my music execution language.

This problem of designing a control discipline for a complicated electronic or mechanical system is what unifies the experimentation with software and hardware that is robotics. It is impossible to build a robot arm which can be the output peripheral of a Chess 4.7 unless one has as good an understanding of the software of motion as one has of the mechanical aspects of motion. It is impossible to verify a simulation of motion which exists in software unless one is willing to build the mechanical system as well. The interaction of the many phases of the mechanical, electronic, and software systems leads to all kinds of opportunity for design error and the feedback process which produces a better design. Just as readers have taken it upon themselves to get into the nitty gritty details of computer systems and software in order to become educated about this exciting technology, I expect to see much more evidence of this experimenting in robotics as time goes on.

In summary, the state of robotics for individuals is a field which is only now beginning. Without the microprocessor innovations that make intelligent machines inexpensive the personal computer would be impossible. And the personal computer, which provides inexpensive software tools for experimentation, is what makes the key part of robots possible: their intelligent operation. It is still a basement or garage activity with respect to engineering of the mechanical portions of a robotic system, as further evidenced by this issue's articles. But science fiction is full of examples to tantalize the willing experimenter to take a chance on creating a real system that works. For the true experimenter, the fun is in the challenge of making science fiction real. The personal computer is an eminently useful component in this form of fun. ■

REFERENCES

Loofbourrow, T, *How to Build a Computer-Controlled Robot,* Hayden Book Company Inc, Rochelle Park NJ, 1978.

Raphael, B, *The Thinking Computer, Mind Inside Matter,* W H Freeman and Company, San Francisco, 1976.

What's New?

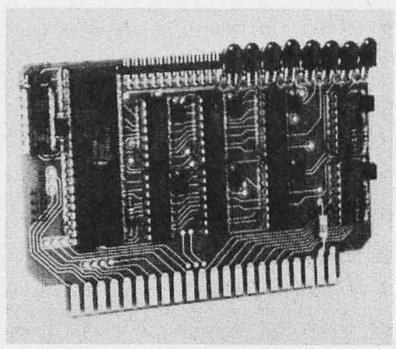
Control Logic Introduces IEEE-488 Bus Interface

Control Logic Inc has announced the addition of a bus for its M Series of modular microcomputers. The MEE-888 is an interface bus (GPIB) that meets the requirements of IEEE Standard 488. The functions of talker, listener and controller may all be accomplished using this interface with the appropriate controlling software. The MEE-888 is contained on a single 3.5 by 4 inch (8.89 by 10.16 cm) card.

The M Series microcomputer uses either the 8080 or Z-80 processor and has up to 64 K bytes of memory in any combination of programmable memory (1 K and 4 K byte boards) and erasable read only memory (2 K byte, 2708 or 8 K byte, 2716). In addition to the IEEE-488 interface, both serial and digital interface boards are offered as well as a complement of analog input and output (IO) with 4 to 20 mA signal conditioning options.

The MEE-888 interface bus is priced at $495. For further information contact Control Logic Inc, Nine Tech Circle, Natick MA 01760. ■

Circle 544 on inquiry card.



Teletek System Central Interface

The System Central Interface (SCI) is designed for use with the S-100 bus. The SCI provides a serial port with RS-232 and 20 mA or 60 mA current loop capabilities and speeds from 45 to 9600 bps; three independent 8 bit parallel ports; a high speed cassette port capable of reading and writing biphase (Tarbell), CUTS, and Kansas City with data speeds from 800 to 100,000 bps; two on board relays for control of two recorders; three status lines to control an automatic tape deck; 256 bytes of programmable memory for stack space and buffer storage; a 2708 programmer; two 2708s with a 2 K byte system monitor program and space for an additional 2708.

Contact Teletek Enterprises Inc, Dept 16, 11505B Douglas Rd, Rancho Cordova CA 95670. ■

Circle 546 on inquiry card.

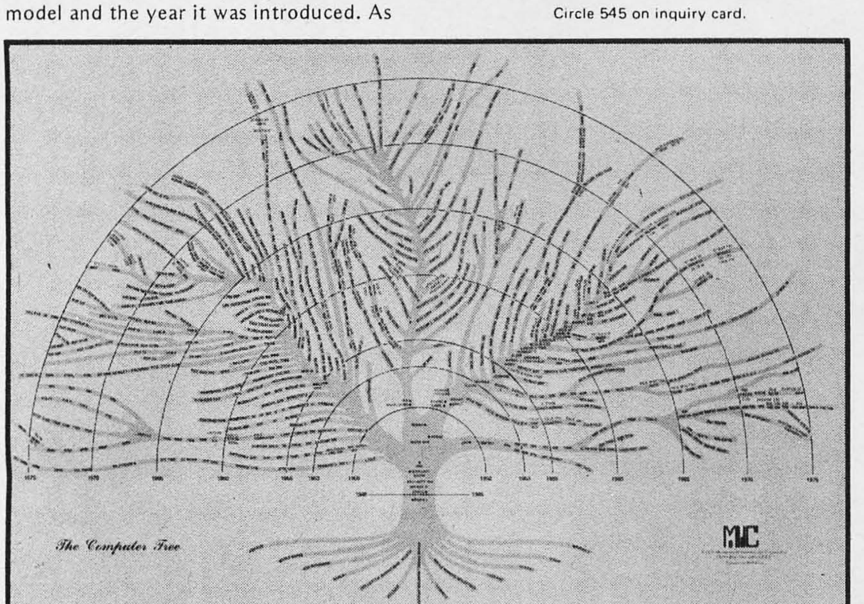
Tracing Computer History

This pictorial evolutionary illustration traces the history of computers through more than 30 years of development. Beginning with the Mark I, the tree branches out to link together each successive generation within a company, forming a continual family structure.

This 18 by 24 inch poster names each model and the year it was introduced. As an example, the tree shows the IBM 607 making its appearance in the 1950s. It branches off to the IBM 7094 in the early 1960s, the IBM System 360 starting in 1965 and the IBM System 370 in the early 1970s.

The poster is available for $10, and outside the United States, for $15. For further information, contact MIC, 140 Barclay Ctr, Cherry Hill NJ 08034. ■

Circle 545 on inquiry card.



8 Digit Panel Display



The Microport 8 is an 8 digit, self-contained, general purpose panel display. Packaged much like a data processing manager, it contains all the timing, memory and multiplexing electronics required for interfacing to an 8 bit microprocessor port (one TTL load). The processor provides the unit with an 8 bit output word only when the display is to be updated (three bits to select the character to be updated, four bits to select the data and one bit to strobe).

Two character fonts, hexadecimal and extended decimal, are provided. Each can be used on either half of the 0.5 inch high LED display.

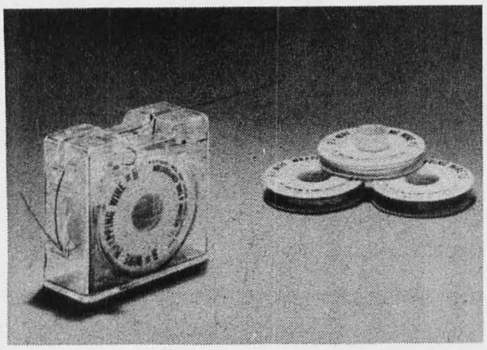
A holder is provided for the user to insert a legend strip or log. 5 V at 800 mA maximum is required.

The price is $109 and the unit can be obtained from Telesis Laboratory, POB 1843, Chillicothe OH 45601. ■

Circle 547 on inquiry card.

What's New?

3 Color Wire Dispenser Cuts and Strips



The WD-30-TRI dispenser from OK Machine and Tool holds three colors of wire and features a built-in cutting and stripping mechanism. The refillable dispenser holds 50 feet (15.2 meters) each of red, white and blue Kynar insulated silver plated solid copper wire. Designed for wire wrapping, this dispenser is also usable for other wiring jobs. The WD-30-TRI is priced at $5.95; the R-30-TRI 3 color refill is $3.95. Contact OK Machine and Tool Corp, 3455 Conner St, Bronx NY 10475.■

Circle 627 on inquiry card.

Service and Repair Manual for Electronic Games



How to Repair Video Games by Robert Goodman is a 270 page service manual containing information on products sold by manufacturers of electronic games. Each chapter of the manual is devoted to an individual manufacturer's equipment. The three integrated circuit manufacturers covered are General Instrument, Texas Instrument and National Semiconductor; equipment manufacturers include Magnavox, Atari, Radio Shack, RCA and Midway. The manual is $7.95 and is available from Tab Books, Blue Ridge Summit PA 17214.■

Circle 628 on inquiry card.

New Flowchart Form Speeds Debugging and Aids Logic Clarity

Flowchartrix is a new flowchart worksheet designed especially for individuals who develop programs for minicomputers and microcomputers. The Flowchartrix 78F2 contains a matrix of 77 logic blocks (seven columns by 11 rows). The 7 by 11 matrix has a central column for executive control logic, plus three columns on each side to describe loops and subroutines. These columns allow room for users to write loops that are laid out visually as loops. Each matrix cell is labeled with an alphanumeric code to give it a reference address when added to the page number in order to help track logic flow from page to page, and give a specific reference to note when actual coding begins. To further speed initial logic development, the 78F2 incorporates special guide marks in every matrix cell to aid in the drawing of most common standard flowchart shapes freehand using a pen or soft pencil.

The 78F2 is 3 hole punch with folding guides designed to fit neatly in a standard 3 ring binder. 50 sheets to the pad, the new forms are available in 2 pad packages, 10 pad boxes, and 43 pad cases. Inquiries should be addressed to Stirling/Bekdorf, 4407 Parkwood, San Antonio TX 78218.■

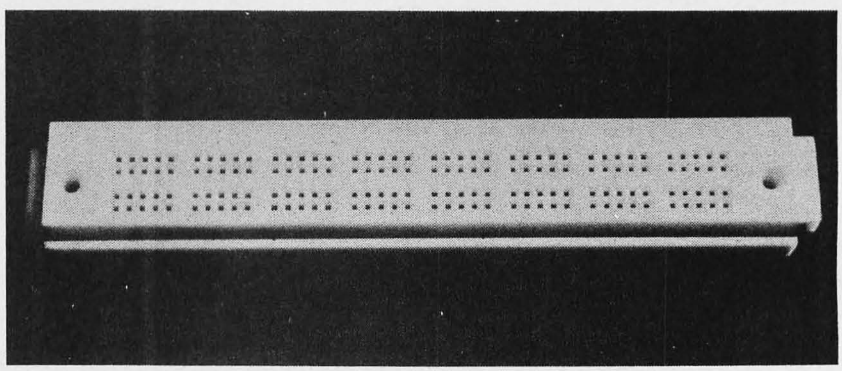
Circle 629 on inquiry card.

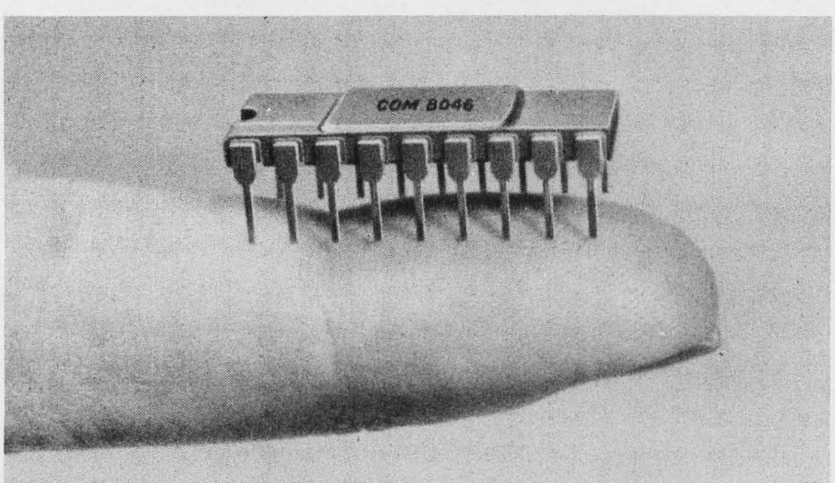
New EXP-4B Quad Bus Strip

The newest member of the Experimentor family, the Model EXP-4B quad bus strip, has been introduced by Continental Specialties Corp, 70 Fulton Ter, New Haven CT 06509.

The EXP-4B adds signal, supply and control line expansion capabilities. The unit is 3/8 by 3/4 inches (0.95 by 1.9 cm) and includes four 40 point bus strips. It also features tongue and groove sides for assembly into interlocked arrays. The EXP-4B is priced at $4.■

Circle 630 on inquiry card.





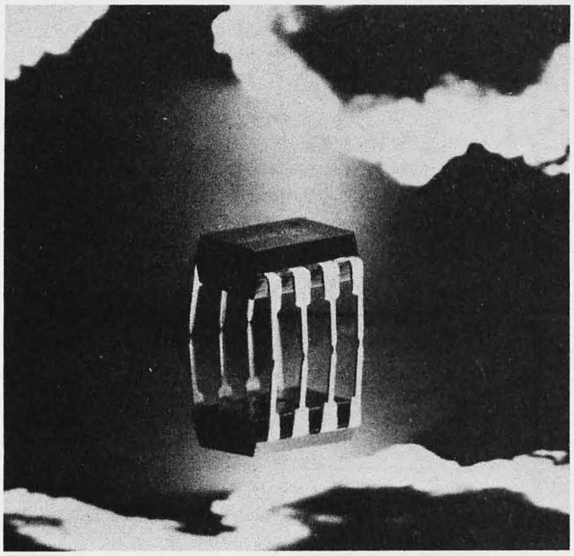
Data Rate Generator Operates with 5 V Power Supply

This Model COM8046 data rate generator is a program divider using depletion mode loads to allow operation from a single +5 V power supply. The COM8046 is dedicated to generating the full spectrum of 16 asynchronous data communication frequencies for 1X, 16X and 32X USART, ASTRO, and USYNRT devices.

The unit contains an on chip crystal oscillator for use in providing the master reference frequency. Alternately, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2.

Contact Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge NY 11787.■

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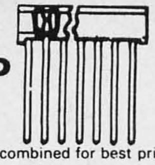
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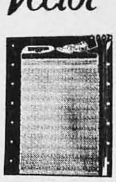
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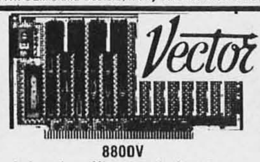
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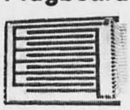


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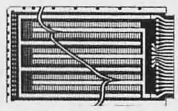
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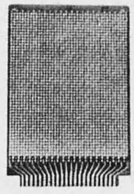
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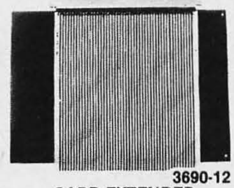
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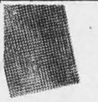


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Card Extender has 100 contacts 50 per side on .125 centers-Attached connector-is compatible with S-100 Bus Systems. **$25.83**
3690 6.5" 22/44 pin .156 ctrs. Extenders $13.17

1/16 Vector BOARD



.042 dia holes on 0.1 spacing for IC's

PART NO.	SIZE	PRICE 1-9	10-19
Phenolic			
64P44XXXP	4.5x6.5"	$1.56	$1.40
169P44XXXP	4.5x17"	$3.69	$3.32
Epoxy Glass			
64P44	4.5x6.5"	$1.79	$1.61
84P44	4.5x8.5"	$2.21	$1.99
169P44	4.5x17"	$4.52	$4.07
169P84	8.5x17"	$8.03	$7.23

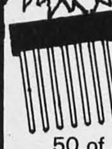
TRS-80 apple II MEMORY EXPANSION KITS

4116's RAMS
(16Kx1 300ns)
8 for $79.95
add $5.00 for new Programming. Jumpers for TRS-80 may also be used for S.D. EXPANDORAM

2708

8K 450 ns
EPROM
FACTORY PRIME
$ 9.00 EA.
25 + *Call For Price*

WOW 14 & 16 PIN GOLD 3 LEVEL WIRE WRAP SOCKETS



14 - G3 100 for **$30.00**
16-G3 100 for **$30.00**
50 of each for **$32.00**
Sockets are End & Side stackable, closed entry

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PANAVISE TILTS, TURNS, AND ROTATES TO ANY POSITION. IT HOLDS YOUR WORK EXACTLY WHERE YOU WANT IT.

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IM-10A List $85.00
SPECIAL
$54.95 with tube

Perfectly balanced fluorescent lighting with precision magnifier lens. Tough thermoplastic shade. Easy lens removal. New wire clip design permits easy installation and removal of fluorescent tube. Comes with plastic shield to protect tube from soiling and damage.
Colors: Gray, Black, and Chocolate Brown. Comes with one 22 watt T-9 Circline fluorescent tube. 3 diopter lens.

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except CA., AK., HI., Call (213) 894-8171

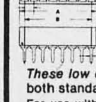
Price Breakthrough! $16.95 or 3/$45.00



MA1003 CAR CLOCK

Bright Green Fluorescent Display Crystal Time Base Assembled, just add switches and 12 VDC.

SPECIAL



14CS2 100 for $14.00
16CS2 100 for $16.00
14 pin CS2 10 for $2.00
16 pin CS2 8 for $2.00

These low cost DIP sockets will accept both standard width plugs and chips.
For use with chips, the sockets offer a low profile height of only .125" above the board. These sockets are end stackable.

Vector WRAP POST

for .042 dia. holes (all boards on this page)
T44/C pkg. 100 .. $ 2.34
T44/M pkg. 1000 ..... $14.35
A-13 hand installing tool .... $ 2.94

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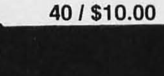
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24 PIN DIP PLUGS WITH COVERS

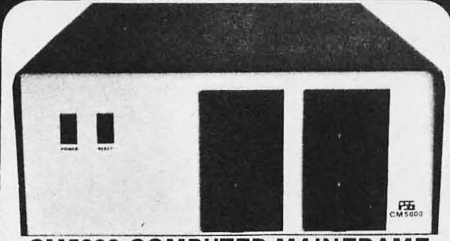


3 / $1.00
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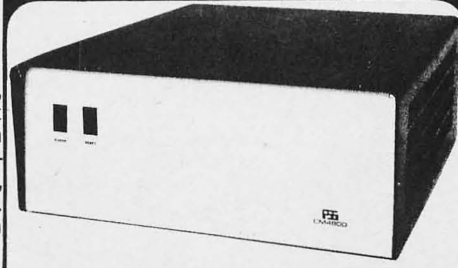
PSS
PROBLEM SOLVER SYSTEMS, INC.



CM5000 COMPUTER MAINFRAME

Includes cabinet, 18 amp power supply, S-100 compatible STREAKER-12® (12-slot motherboard), and dual-disk provision with disk power supply. The CM5000 is fan-cooled, has AC line filter to eliminate EMI, and is fully-assembled and factory-tested. Power and reset switches are located on front panel.

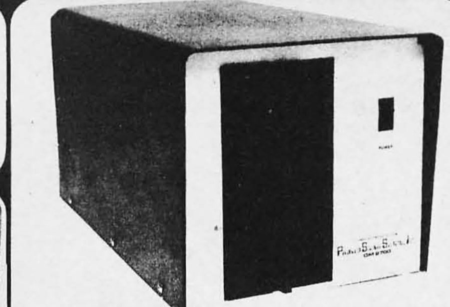
$549.00*



CM4800 COMPUTER MAINFRAME

Includes cabinet, 30 amp power supply, and the S-100 compatible STREAKER-22® (22-slot motherboard). The CM4800 is fan-cooled, has AC line filter to eliminate EMI, and is fully-assembled and factory-tested. Power and reset switches are located on front panel. OPTION: Model CM4800D—includes provision for floppy disk power supply. Also available: Model CM4900—with 18 amp power supply and STREAKER-12® (12-slot motherboard)

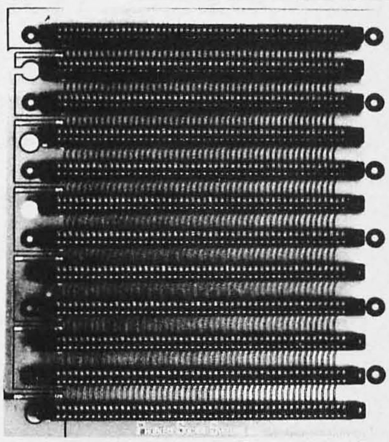
$549.00*



DM2700 DISK CABINET WITH POWER SUPPLY

Accepts either PerSci or Shugart mini-floppy disks. Includes data cable and AC line filter to eliminate EMI. Operates from 100 to 125 volts or 200 to 250 volts, 50 or 60Hz. Fully assembled and tested at factory. (Disk drive not included). OPTION: Model DM2700S—Includes Shugart Series 800 minifloppy disk.

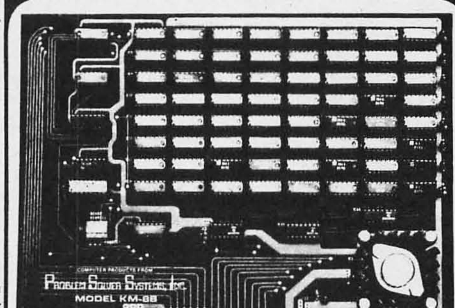
$249.00*



STREAKER® MOTHERBOARDS

- In 7, 12, and 22-slot versions • S-100 compatible
- Connectors have bifurcated, gold-plated contacts
- Ground plane surrounding each signal
- Compatible with Imsai chassis
- Power connections compatible with power supplies in PSS's CM4800, CM5000, and CM5200 Computer mainframes.
- Fully-assembled and tested at factory
- No isolation hardware required for mounting.

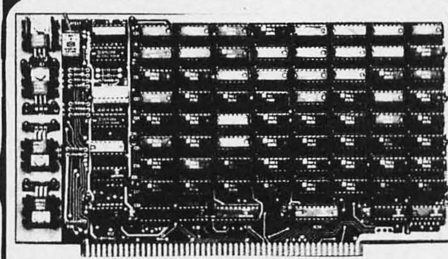
Streaker 7	**$79.95**
Streaker 12	**$99.00**
Streaker 22	**$159.00**



KM8B / KIM-4® COMPATIBLE

- KIM® compatible, 8K x 8 bit static RAM
- Can be connected directly to KIM-1®
- Plugs directly into KIM-4® motherboard • 2MHz
- Addressable in 8K steps
- Allows expansion of KIM® computer up to 65K of memory
- Memory protection activated / deactivated by DIP Switch
- Buffered address and data lines
- Operates from either an unregulated 8 volt or a regulated 5 volt power supply
- All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory.

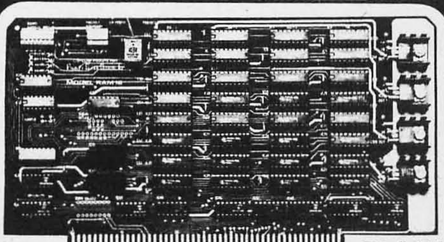
$179.00



RAM 8 $199.00

- S-100, 8K x 8 bit static RAM
- 4MHz
- Addressable in 8K steps
- Memory protection in 1K increments, from bottom board address up or top down
- Memory protection activated / deactivated by large, easily accessible switch
- May deactivate up to six 1K segments of board by use of jumpers to create "holes" for other devices
- DIP switch selectable wait states
- Phantom line jumper
- Schmitt trigger-buffered I/O lines
- All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory.

OPTION: RAM8B—2MHz **$179.00**



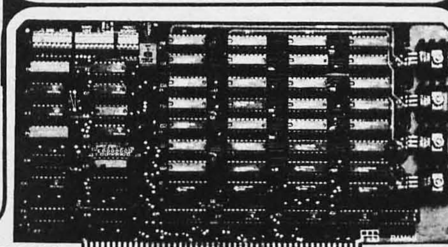
RAM 16 $449.00

- S-100, 16K x 8 bit static RAM • 4MHz
- Addressable in 4K steps
- Memory protection in 1K increments, from bottom board address up or top down
- Memory protection activated / deactivated by large, easily accessible switch
- May deactivate up to six 1K segments of board by use of jumpers to create "holes for other devices
- DIP switch selectable wait states
- Phantom line DIP switch
- Bank-select for expansion beyond 65K of memory
- Schmitt trigger-buffered I/O lines
- All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factotry

OPTION: RAM16B—2MHz

$429.00

*Please include sufficient funds to cover cost of shipping of Mainframes.



RAM 65 $495.00

- S-100, 16K x 8 bit static RAM • 4MHz
- Addressable in 4K steps
- Memory protection in 1K increments, from bottom board address up or top down
- Memory protection activated / deactivated by large, easily accessible switch
- May deactivate up to six 1K segments of board by use of jumpers to create "holes" for other devices
- DIP switch selectable wait states
- Phantom line DIP switch
- Features bank selection by I/O instruction using any one of 256 DIP switch-selectable codes—allows up to 256 software-controlled memory banks.
- Schmitt trigger-buffered I/O lines • All IC's mounted in low-profile sockets
- Assembled, tested, burned-in at factory

OPTION: RAM65B—2MHz

$459.00

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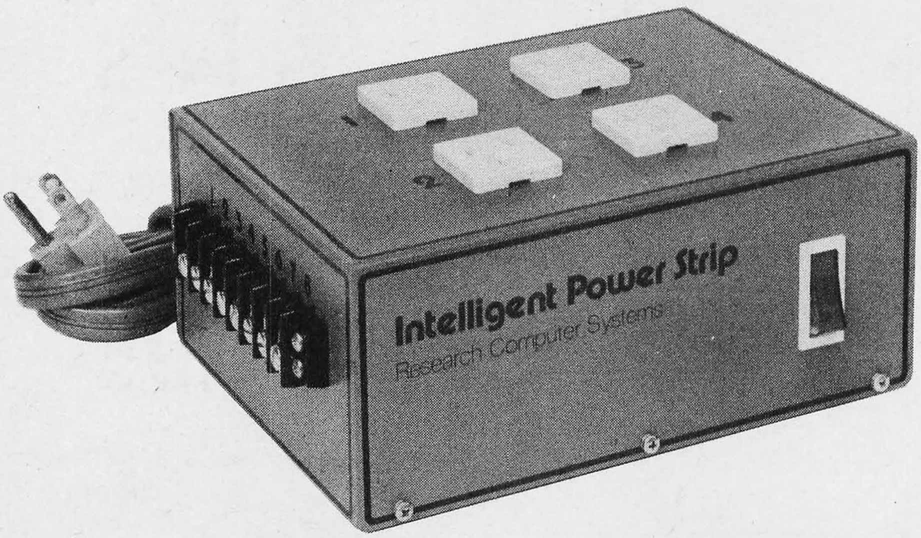
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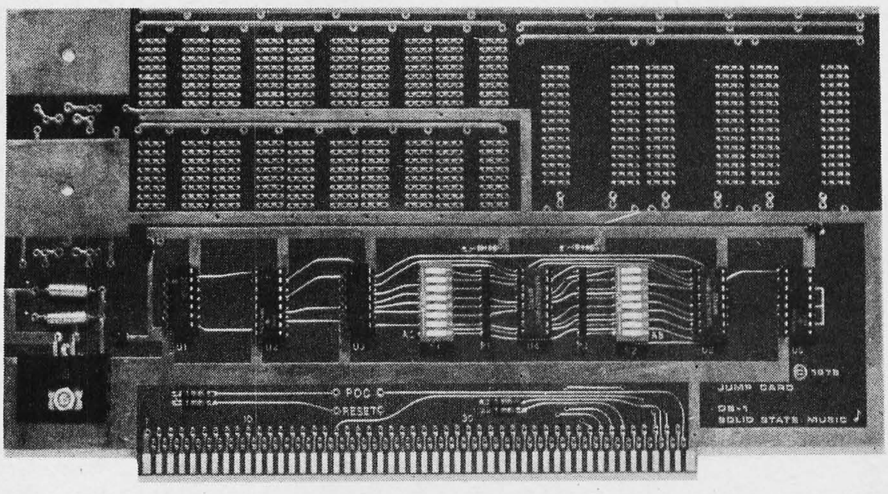
Intelligent Power Strip Controls up to Four Power Devices



The Intelligent Power Strip (IPS) allows a computer to control up to four high power devices. Transistor-transistor logic (TTL) level lines make interfacing with a computer easy. The IPS allows phase control, letting software control motor speeds and dim lights. It also allows on and off control and random or zero voltage switching of all common household appliances. Using one of the power outlets, the driving computer can turn itself off. All inputs from the computer are optically coupled to protect the computer hardware. Full protection against power failure and voltage surges is also provided. The Intelligent Power Strip sells for $129.50 and comes fully assembled with a 5 foot power cord and an applications manual. Contact Research Computer Systems, POB 1214, Richardson TX 75080.■

Circle 551 on inquiry card.

New Vector Jump and Prototype Board



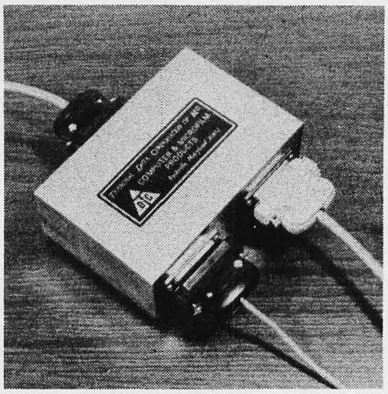
The OB-1 board is a vector jump and prototyping board that is plug compatible with all S-100 bus mainframes. The board has a full 16 bits of vector jump address and can jump to any individual addressable location. Additional features of the OB-1 include prototyping areas on the board for ten 16 pin integrated circuits, three 24 or 28 pin integrated circuits, plus two spare regulator patterns.

The OB-1 will work with or without phantom disable, and can be set to jump on power on clear, reset, or both. The board includes gold plated edge connector contacts, and TI low profile sockets.

The price for the OB-1 is $54.95. For further information contact SSM, 2116 Walsh Av, Santa Clara CA 95050.■

Circle 554 on inquiry card.

Data Splitter Kit



Terminal Data Corporation has made its Model 1200 RS-232 Data Splitter available in kit form. The Model 1200 gives the video terminal user a second interface for a printer, plotter, cassette or tape drive. It operates at any speed and isolates the two output devices from each other, while providing two RS-232 interfaces from the terminal.

The kit consists of three RS-232 connectors, printed circuit board, all necessary components, enclosure, mounting hardware and assembly instructions. It is priced at $49 and can be obtained by writing the company at 11878 Coakley Cir, Rockville MD 20852.■

Circle 552 on inquiry card.

Tape Signal Conditioning Unit Makes Program Loading Easier

The Futureworld FW-100 tape signal conditioning unit features generation of saturated rectangular waveforms from noisy cassettes (the unit will tolerate at least 5 decibels of dropout) and works equally well with low (TRS-80) or high (Apple, Tarbell, etc) transmission rates. It is contained in a small, insulated potted module which measures 9.84 by 11.81 by 3.94 inches (25 by 30 by 10 cm). Four wires connect to the supply voltage, input, output and ground. The unit uses all CMOS circuitry and operates from +4 V to +9 V; current drain is less than 1 mA when operated from a +5 V supply. It may be installed inside the computer if desired.

The FW-100 is priced at $7.69 and is available from Futureworld Personal Systems Store, POB 2252, Chapel Hill NC 27514. ■

Circle 553 on inquiry card.

Desk with Slide Out Card Cage

An attractively styled desk with slide out card cage and power supply rack has been introduced by RD Electronics, POB 243, Richfield Springs NY 13439. Plug-in power line filters, power supplies and blank cards are available.

RD Electronics carries a complete line of electronic components, power supplies and accessories for the personal computer user.■

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LX303

ALL THE MOST WANTED FEATURES AT A MOST WANTED PRICE . . .

BIG ½" HIGH LCD DISPLAY

USE INDOORS OR OUT

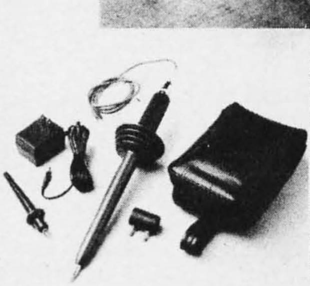
200 HOUR 9V BATTERY LIFE

AUTO ZERO, POLARITY, OVERRANGE INDICATION





Removable cover stores test lead set furnished as part of the unit.



Available Accessories

RC-3 115V AC Adapter	$7.50
CC-3 Deluxe Padded Vinyl Carrying Case	$7.50
VP-10 X10 DCV Probe Adapter/ Protector 10Kv	$14.95
VP-40 40Kv DC Probe	$35.00
CS-1 10 Amp Current Shunt	$14.95

$74.95

100 mV DC F.S. SENSITIVITY

19 RANGES AND FUNCTIONS

Here is the handfull of accuracy you've been waiting for. Handsomely encased. Compact. Efficient. Only 8 ounces. Hickok's exciting, new LX 303, 3½ digit Mini-Multimeter with high quality components, one year guarantee and rugged Cycolac® case offers features previously found only in expensive units . . . at a price under $75.00! So why wait any longer? The amazing LX 303 is here, NOW! Another American made test equipment breakthrough from Hickok.

SPECIFICATIONS

DC VOLTS (5 RANGES): 0.1mV to 1000V; Accuracy ±0.5% rdg ±0.5% f.s.; Input imped: 10MΩ; Max. input 1kV except 500V on 200mV range.
AC VOLTS (40Hz to 5kHz): 0.1V to 600V; Accuracy: ±1.0% rdg ±0.5% f.s. (—2dB max. at 5kHz); Max. input: 600V.
RESISTANCE (6 LOW POWER RANGES): 0.1Ω to 20MΩ; Accuracy: ±.05% rdg ±0.5% f.s. (±1.5% rdg on 20MΩ range); input protected to 120VAC all ranges.
DC CURRENT (6 RANGES): .01nA to 100mA; Accuracy: ±1.0% rdg ±0.5% f.s.
DIMENSIONS AND WEIGHT: 5-7/8" x 3-3/8" x 1-3/4", 8 oz.; POWER: 9V battery (not included) or Hickok AC adapter; READ RATE: 3/sec.

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7400 TTL

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		SN7472N	.29		
SN7400N	.16	SN7473N	.35	SN74160N	.89
SN7401N	.18	SN7474N	.35	SN74161N	.89
SN7402N	.18	SN7475N	.49	SN74162N	1.95
SN7403N	.18	SN7476N	.35	SN74163N	.89
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SN7411N	.25	SN7490N	.45	SN74174N	.89
SN7412N	.25	SN7491N	.59	SN74175N	.79
SN7413N	.40	SN7492N	.43	SN74176N	.79
SN7414N	.70	SN7493N	.43	SN74177N	.79
SN7416N	.25	SN7494N	.65	SN74179N	1.95
SN7417N	.25	SN7495N	.65	SN74180N	.79
SN7420N	.20	SN7496N	.65	SN74181N	1.95
SN7421N	.29	SN7497N	3.00	SN74182N	.79
SN7422N	.39	SN74100N	.89	SN74184N	1.95
SN7423N	.25	SN74107N	.35	SN74185N	1.95
SN7425N	.29	SN74109N	.59	SN74186N	9.95
SN7426N	.29	SN74116N	1.95	SN74188N	3.95
SN7427N	.25	SN74121N	.35	SN74190N	1.25
SN7429N	.39	SN74122N	.39	SN74191N	1.25
SN7430N	.20	SN74123N	.49	SN74192N	.79
SN7432N	.25	SN74125N	.49	SN74193N	.79
SN7437N	.25	SN74126N	.49	SN74194N	.89
SN7438N	.25	SN74132N	.75	SN74195N	.69
SN7439N	.25	SN74136N	.75	SN74196N	.89
SN7440N	.20	SN74141N	.79	SN74197N	.89
SN7441N	.89	SN74142N	2.95	SN74198N	1.49
SN7442N	.49	SN74143N	2.95	SN74199N	1.49
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SN7445N	.75	SN74147N	1.95	SN74279N	.79
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SN7447N	.59	SN74150N	.89	SN74284N	3.95
SN7448N	.79	SN74151N	.59	SN74285N	3.95
SN7450N	.20	SN74152N	.59	SN74365N	.69
SN7451N	.20	SN74153N	.59	SN74366N	.69
SN7453N	.20	SN74154N	.99	SN74367N	.69
SN7454N	.20	SN74155N	.79	SN74368N	.69
SN7459A	.25	SN74156N	.79	SN74390N	1.95
SN7460N	.20	SN74157N	.65	SN74393N	1.95

20% Discount 100 pcs combined order 25% -1000 pcs combined order

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CD4000	.23			CD4070	.55
CD4001	.23			CD4071	.23
CD4002	.23	CD4028	.89	CD4072	.49
CD4006	1.19	CD4029	1.19	CD4076	1.39
CD4007	.25	CD4030	.49	CD4081	.23
CD4009	.49	CD4035	.99	CD4082	.23
CD4010	.49	CD4040	1.19	CD4093	.99
CD4011	.23	CD4041	1.25	CD4098	2.49
CD4012	.25	CD4042	.99	MC14409	14.95
CD4013	.39	CD4043	.89	MC14410	14.95
CD4014	1.39	CD4044	.89	MC14411	14.95
CD4015	1.19	CD4046	1.79	MC14419	4.95
CD4016	.49	CD4047	2.50	MC14433	19.95
CD4017	1.19	CD4048	1.35	MC14506	.75
CD4018	.99	CD4049	.49	MC14507	.99
CD4019	.49	CD4050	.49	MC14562	14.50
CD4020	1.19	CD4051	1.19	MC14583	3.50
CD4021	1.39	CD4053	1.19	CD4508	3.95
CD4022	1.19	CD4056	2.95	CD4510	1.39
CD4023	.23	CD4059	9.95	CD4511	1.29
CD4024	.79	CD4060	1.49	CD4515	2.95
CD4025	.23	CD4066	.79	CD4518	1.29
CD4026	2.25	CD4068	.39	CD4520	1.29
CD4027	.69	CD4069	.45	CD4566	2.25

74C00

74C00	.39			74C163	2.49
74C02	.39			74C164	2.49
74C04	.39	74C85	2.49	74C173	2.60
74C08	.49	74C90	1.95	74C192	2.49
74C10	.39	74C93	1.95	74C193	2.49
74C14	1.95	74C95	1.95	74C195	2.49
74C20	.39	74C107	1.25	74C922	5.95
74C30	.39	74C151	2.90	74C923	6.25
74C42	1.95	74C154	3.00	74C925	8.95
74C48	2.49	74C157	2.15	74C926	8.95
74C73	.89	74C160	2.49	80C95	1.50
74C74	.89	74C161	2.49	80C97	1.50

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78MG	1.75			LM710N	.79
LM106H	.99			LM711N	.39
LM300H	.80	LM340K-18	1.35	LM723N/H	.55
LM301CN/H	.35	LM340K-24	1.35	LM733N	1.00
LM302H	.75	LM340T-5	1.25	LM739N	1.19
LM304H	1.00	LM340T-6	1.25	LM741CN/H	.35
LM305H	.60	LM340T-8	1.25	LM741-14N	.39
LM307CN/H	.35	LM340T-12	1.25	LM747N/H	.79
LM308CN/H	1.00	LM340T-15	1.25	LM748N/H	.39
LM309H	1.10	LM340T-18	1.25	LM1310N	2.95
LM309K	1.25	LM340T-24	1.25	LM1458CN/H	.59
LM310CN	1.15	LM358N	1.00	MC1488N	1.95
LM311N/H	.90	LM370N	1.95	MC1489N	1.95
LM312H	1.95	LM373N	3.25	LM1496N	.95
LM317K	6.50	LM377N	4.00	LM1556V	1.75
LM318CN/H	1.50	LM380N	1.25	MC1741SCP	3.00
LM319N	1.30	LM380CN	.99	LM2111N	1.95
LM320K-5	1.35	LM381N	1.79	LM2901N	2.95
LM320K-5.2	1.35	LM382N	1.79	LM3053N	1.50
LM320K-12	1.35	NE501N	8.00	LM3065N	1.49
LM320K-15	1.35	NE510A	6.00	LM3900N(3401)	.49
LM320K-18	1.35	NE529A	4.95	LM3905N	.89
LM320K-24	1.35	NE531H/V	3.95	LM3909N	1.25
LM320T-5	1.25	NE536T	6.00	MC5558V	.59
LM320T-5.2	1.25	NE540L	6.00	8038B	4.95
LM320T-8	1.25	NE544N	4.95	LM75450N	.49
LM320T-12	1.25	NE550N	1.30	75451CN	.39
LM320T-15	1.25	NE555V	.39	75452CN	.39
LM320T-18	1.25	NE556N	.99	75453CN	.39
LM320T-24	1.25	NE560B	5.00	75454CN	.39
LM323K-5	5.95	NE561B	5.00	75491CN	.79
LM324N	1.80	NE562B	5.00	75492CN	.89
LM339N	.99	NE565N/H	1.25	75493N	.89
LM340K-5	1.35	NE566CN	1.75	75494CN	.89
LM340K-6	1.35	NE567V/H	.99	RC4136	1.25
LM340K-8	1.35	NE570N	4.95	RC4151	5.95
LM340K-12	1.35	LM703CN/H	.69	RC4194	5.95
LM340K-15	1.35	LM709N/H	.29	RC4195	4.49

74LS00TTL

74LS00	.23			74LS138	.69
74LS01	.23			74LS139	.69
74LS02	.23	74LS47	.69	74LS151	.69
74LS03	.23	74LS51	.23	74LS155	.69
74LS04	.29	74LS54	.23	74LS157	.69
74LS05	.29	74LS55	.23	74LS160	.89
74LS08	.23	74LS73	.35	74LS161	.89
74LS09	.29	74LS74	.35	74LS162	.89
74LS10	.23	74LS75	.49	74LS163	.89
74LS11	.60	74LS76	.35	74LS164	.99
74LS13	.49	74LS78	.39	74LS175	.79
74LS14	.99	74LS83	.75	74LS181	2.49
74LS15	.29	74LS85	.99	74LS190	.89
74LS20	.23	74LS86	.35	74LS191	.89
74LS21	.29	74LS90	.49	74LS192	.89
74LS22	.29	74LS92	.59	74LS193	.89
74LS26	.29	74LS93	.59	74LS194	.89
74LS27	.29	74LS95	.79	74LS195	.89
74LS28	.29	74LS96	.89	74LS253	.79
74LS30	.23	74LS107	.35	74LS257	.69
74LS32	.29	74LS109	.35	74LS258	1.39
74LS37	.35	74LS112	.35	74LS260	.55
74LS40	.29	74LS123	.99	74LS279	.59
74LS42	.69	74LS125	.69	74LS367	.59
		74LS132	.79	74LS368	.59
		74LS136	.39	74LS670	1.95

Jameco ELECTRONICS (New) Kits

a division of JAMES ELECTRONICS of California

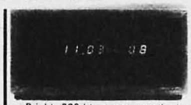
Digital Stopwatch Kit



- Use Intersil 7205 Chip
- Plated thru double-sided P.C. Board
- LED display (red)
- Times to 59 min. 59.59 sec. with auto reset
- Quartz crystal controlled
- Three stopwatches in one: single event, split (cummulative) and taylor (sequential timing)
- Uses 3 penlite batteries
- Size: 4.5" x 2.15" x .90"

JE900 $39.95

6-Digit Clock Kit



- Bright .300 ht. common cathode display
- Uses MM5314 clock chip
- Switches for hours, minutes and hold functions
- Hours easily viewable to 20 feet
- Simulated walnut case
- 115 VAC operation
- 12 or 24 hour operation
- Includes all components, case and wall transformer
- Size: 6-3/4" x 3-1/8" x 1-3/4"

JE701 $19.95

ALSO AVAILABLE:

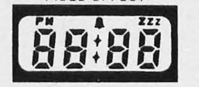
JE200 5v lamp power supply $14.95 JE2206B Function Generator $19.95
JE730 4-digit clock kit 14.95 JE747 Jumbo 6-digit clock kit 29.95

DISCRETE LEDS

.200" dia.			.125" dia.		
XC556R	red	5/$1	XC209R	red	5/$1
XC556G	green	4/$1	XC209G	green	4/$1
XC556Y	yellow	4/$1	XC209Y	yellow	4/$1
XC556C	clear	4/$1			
.200" dia.			.185" dia.		
XC22R	red	5/$1	XC526R	red	5/$1
XC22G	green	4/$1	XC526G	green	4/$1
XC22Y	yellow	4/$1	XC526Y	yellow	4/$1
.170" dia.			XC526C	clear	4/$1
MV10B	red	4/$1	.190" dia.		
.085" dia.			XC111R	red	5/$1
MV50	red	6/$1	XC111G	green	4/$1
INFRA-RED LED 1/4"x1/4"x1/16" flat		5/$1	XC111Y	yellow	4/$1
			XC111C	clear	4/$1

TIMEX T1001 LIQUID CRYSTAL DISPLAY

FIELD EFFECT



4 DIGIT — .5" CHARACTERS
THREE ENUNCIATORS
2.00" X 1.20" PACKAGE
INCLUDES CONNECTOR

T1001-Transmissive $7.95
T1001A-Reflective 8.25

DISPLAY LEDS

TYPE	POLARITY	HT	PRICE	TYPE	POLARITY	HT	PRICE
MAN 1	Common Anode-red	.270	2.95	MAN 6730	Common Anode-red ± 1	.560	.99
MAN 2	5 x 7 Dot Matrix-red	.300	4.95	MAN 6740	Common Cathode-red-D.D.	.560	.99
MAN 3	Common Cathode-red	.125	.25	MAN 6750	Common Cathode-red ± 1	.560	.99
MAN 4	Common Cathode-red	.187	1.95	MAN 6760	Common Anode-red	.560	.99
MAN 7G	Common Anode-green	.300	1.25	MAN 6780	Common Cathode-red	.560	.99
MAN 7Y	Common Anode-yellow	.300	.99	DL701	Common Anode-red ± 1	.300	.99
MAN 72	Common Anode-red	.300	.99	DL704	Common Cathode-red	.300	.99
MAN 74	Common Cathode-red	.300	1.25	DL707	Common Anode-red	.300	.99
MAN 82	Common Anode-yellow	.300	.99	DL728	Common Cathode-red	.500	1.49
MAN 84	Common Cathode-yellow	.300	.99	DL741	Common Anode-red	.600	1.25
MAN 3620	Common Anode-orange	.300	.99	DL746	Common Anode-red ± 1	.630	1.49
MAN 3630	Common Anode-orange ± 1	.300	.99	DL747	Common Anode-red	.600	1.49
MAN 3640	Common Cathode-orange	.300	.99	DL749	Common Cathode-red ± 1	.630	1.49
MAN 4610	Common Anode-orange	.300	.99	DL750	Common Cathode-red	.600	1.49
MAN 4640	Common Cathode-orange	.400	.99	DL338	Common Cathode-red	.110	.35
MAN 4710	Common Anode-red	.400	.99	FND70	Common Cathode	.250	.69
MAN 4730	Common Anode-red ± 1	.400	.99	FND358	Common Cathode ± 1	.357	.99
MAN 4740	Common Cathode-red	.400	.99	FND359	Common Cathode	.357	.75
MAN 4810	Common Anode-yellow	.400	.99	FND503	Common Cathode(FND500)	.500	.99
MAN 4840	Common Cathode-yellow	.400	.99	FND507	Common Anode (FND510)	.500	.99
MAN 6610	Common Anode-orange-D.D.	.560	.99	5082-7730	Common Anode-red	.300	1.30
MAN 6630	Common Anode-orange ± 1	.560	.99	HDSP-3400	Common Anode-red	.800	2.10
MAN 6640	Common Cathode-orange-D.D.	.560	.99	HDSP-3403	Common Cathode red	.800	2.10
MAN 6650	Common Cathode-orange ± 1	.560	.99	5082-7300	4 x 7 sgl. Digit-RHDP	.600	19.95
MAN 6660	Common Anode-orange	.560	.99	5082-7302	4 x 7 Sgl. Digit-LHDP	.600	19.95
MAN 6680	Common Cathode-orange	.560	.99	5082-7304	Overrange character (±1)	.600	15.00
MAN 6710	Common Anode-red-D.D.	.560	.99	5082-7340	4 x 7 Sgl. Digit-Hexadecimal	.600	22.50

RCA LINEAR

CA3013T	2.15	CA3082N	2.00
CA2023T	2.56	CA3083N	1.60
CA3035T	2.48	CA3086N	.85
CA3039T	1.35	CA3089N	3.75
CA3046N	1.30	CA3130T	1.39
CA3059N	3.25	CA3140T	1.25
CA3060N	3.25	CA3160T	1.25
CA3080T	.85	CA3401N	.49
CA3081N	2.00	CA3600N	3.50

CALCULATOR CHIPS/DRIVERS

MM5725	$2.95
MM5738	2.95
DM8864	2.00
DM8865	1.00
DM8887	.75
DM8889	.75
9374 7 seg. C.A. LED driver	

CLOCK CHIPS

MM5309	$4.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5387/1998A	4.95
MM5841	9.95

MOTOROLA

MC1408L7	$4.95
MC1408L8	5.75
MC1439L	2.95
MC3022P	2.95
MC3061P	3.50
MC4016(74416)	7.50
MC4024P	3.95
MC4040P	6.95
MC4044P	4.50

IC SOLDERTAIL — LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin LP	$.17	.16	.15	22 pin LP	$ .37	.36	.35
14 pin LP	.20	.19	.18	24 pin LP	.38	.37	.36
16 pin LP	.22	.21	.20	28 pin LP	.45	.44	.43
18 pin LP	.29	.28	.27	36 pin LP	.60	.59	.58
20 pin LP	.34	.32	.30	40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100		1-24	25-49	50-100
14 pin ST	$.27	.25	.24	28 pin ST	$ .99	.90	.81
16 pin ST	.30	.27	.25	36 pin ST	1.39	1.26	1.15
18 pin ST	.35	.32	.30	40 pin ST	1.59	1.45	1.30
24 pin ST	.49	.45	.42				

SOLDERTAIL STANDARD (GOLD)

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin SG	$.30	.27	.24	24 pin SG	$ .70	.63	.57
14 pin SG	.35	.32	.29	28 pin SG	1.10	1.00	.90
16 pin SG	.38	.35	.32	36 pin SG	1.65	1.40	1.26
18 pin SG	.52	.47	.43	40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin WW	$.39	.38	.31	22 pin WW	$ .95	.85	.75
10 pin WW	.45	.41	.37	24 pin WW	1.05	.95	.85
14 pin WW	.39	.38	.37	28 pin WW	1.40	1.25	1.10
16 pin WW	.43	.42	.41	36 pin WW	1.59	1.45	1.30
18 pin WW	.75	.68	.62	40 pin WW	1.75	1.55	1.40

1/4 WATT RESISTOR ASSORTMENTS – 5%

ASST. 1	5 ea.	10 OHM, 27 OHM	12 OHM, 33 OHM	15 OHM, 39 OHM	18 OHM, 47 OHM	22 OHM, 56 OHM	50 PCS	$1.75
ASST. 2	5 ea.	68 OHM, 180 OHM	82 OHM, 220 OHM	100 OHM, 270 OHM	120 OHM, 330 OHM	150 OHM, 390 OHM	50 PCS	1.75
ASST. 3	5 ea.	470 OHM, 1.2K	560 OHM, 1.5K	680 OHM, 1.8K	820 OHM, 2.2K	1K, 2.7K	50 PCS	1.75
ASST. 4	5 ea.	3.3K, 8.2K	3.9K, 10K	4.7K, 12K	5.6K, 15K	6.8K, 18K	50 PCS	1.75
ASST. 5	5 ea.	22K, 56K	27K, 68K	33K, 82K	39K, 100K	47K, 120K	50 PCS	1.75
ASST. 6	5 ea.	150K, 390K	180K, 470K	220K, 560K	270K, 680K	330K, 820K	50 PCS	1.75
ASST. 7	5 ea.	1M, 2.7M	1.2M, 3.3M	1.5M, 3.9M	1.8M, 4.7M	2.2M, 5.6M	50 PCS	1.75

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) **$9.95 ea.**

$5.00 Minimum Order – U.S. Funds Only
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NEW 1979 Catalog

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a division of JAMES ELECTRONICS of California

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AY-5-9100	Push Button Telephone Dialler	$14.95
AY-5-9200	Repertory Dialler	14.95
AY-5-9500	CMOS Clock Generator	4.95
AY-5-2376	Keyboard Encoder (88 keys)	14.95
HD0165	Keyboard Encoder (16 keys)	7.95
74C922	Keyboard Encoder (16 keys)	9.95

ICM CHIPS

ICM7045	CMOS Precision Timer	24.95
ICM7205	CMOS LED Stopwatch/Timer	19.95
ICM7207	Oscillator Controller	7.50
ICM7208	Seven Decade Counter	19.95
ICM7209	Clock Generator	6.95

NMOS READ ONLY MEMORIES

MCM6571	128 X 9 X 7 ASCII Shifted with Greek	13.50
MCM6574	128 X 9 X 7 Math Symbol & Pictures	13.50
MCM6575	128 X 9 X 7 Alphanumeric Control Character Generator	13.50

MISCELLANEOUS

TL074CN	Quad Low Noise bi-fet Op Amp	2.49
TL494CN	Switching Regulator	4.49
TL496CP	Single Switching Regulator	1.75
11C90	Divide 10/11 Prescaler	19.95
95H90	Hi-Speed Divide 10/11 Prescaler	11.95
4N33	Photo-Darlington Opto-Isolator	3.95
MK50240	Top Octave Freq. Generator	17.50
DS0026CH	5Mhz 2-phase MOS clock driver	3.75
TIL308	.27" red num. display w/integ. logic chip	10.50
MM5320	TV Camera Sync. Generator	14.95
MM5330	4½ Digit DPM Logic Block	5.95
LD110/111	3½ Digit A/D Converter Set	25.00/set

LITRONIX ISO-LIT 1
Photo Transistor Opto-Isolator
(Same as MCT 2 or 4N25)
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Generates Complex Sounds
Low Power - Programmable
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AY-3-8500-1 and 2.01 MHZ Crystal (Chip & Crystal includes score display, 6 games and select angles, etc. **7.95/set**

EXAR

XR205	$3.40			XR2242CP	1.50
XR210	4.40			XR2264	4.25
XR215	4.40			XR2556	3.20
XR320	1.55	JE2206KA	14.95	XR2567	2.99
XR-L555	1.50	JE2206KB	19.95	XR3403	1.25
XR555	.39	XR1800	3.20	XR4136	1.25
XR556	.99	XR2206	4.40	XR4151	2.85
XR567CP	.99	XR2207	3.85	XR4194	1.45
XR567CT	1.25	XR2208	5.20	XR4202	3.60
XR1310P	1.30	XR2209	1.75	XR4212	2.05
XR1468CN	3.85	XR2211	5.25	XR4558	.75
XR1488	1.39	XR2212	4.35	XR4739	1.15
XR1489	1.39	XR2240	3.45	XR4741	1.47

DIODES

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
				1N4002	100 PIV	1 AMP	12/1.00
				1N4003	200 PIV	1 AMP	12/1.00
1N746	3.3	400m	4/1.00	1N4004	400 PIV	1 AMP	12/1.00
1N751	5.1	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N754	6.8	400m	4/1.00	1N3600	50	200m	6/1.00
1N757	9.0	400m	4/1.00	1N4148	75	10m	15/1.00
1N759	12.0	400m	4/1.00	1N4154	35	10m	12/1.00
1N959	8.2	400m	4/1.00	1N4305	75	25m	15/1.00
1N965	15	400m	4/1.00	1N4734	5.6	1w	28
1N5232	5.6	500m	28	1N4735	6.2	1w	28
1N5234	6.2	500m	28	1N4736	6.8	1w	28
1N5235	6.8	500m	28	1N4738	8.2	1w	28
1N5236	7.5	500m	28	1N4742	12	1w	28
1N5242	12	500m	28	1N4744	15	1w	28
1N5245	15	500m	28	1N1183	50 PIV	35 AMP	1.60
1N456	25	40m	6/1.00	1N1184	100 PIV	35 AMP	1.70
1N458	150	7m	6/1.00	1N1185	150 PIV	35 AMP	1.70
1N485A	180	10m	5/1.00	1N1186	200 PIV	35 AMP	1.80
1N4001	50 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR(2N1849)	$1.95
C38M	35A @ 600V	SCR	1.95
2N2328	1.6A @ 300V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC.	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC.	1.95

TRANSISTORS

C106B1	.50			2N3904	4/1.00
MPSA05	.30	2N3055	.89	2N3905	4/1.00
MPSA06	5/1.00	MJE3055	1.00	2N3906	4/1.00
TIS97	6/1.00	2N3392	5/1.00	2N4013	3/1.00
TIS98	6/1.00	2N3398	5/1.00	2N4123	6/1.00
40409	1.75	PN3567	3/1.00	PN4249	4/1.00
40410	1.75	PN3568	4/1.00	PN4250	4/1.00
40673	1.75	PN3569	4/1.00	2N4400	4/1.00
2N918	4/1.00	MPS3638A	5/1.00	2N4401	4/1.00
2N2219A	2/1.00	MPS3702	5/1.00	2N4402	4/1.00
2N2221A	4/1.00	2N3704	5/1.00	2N4403	4/1.00
2N2222A	5/1.00	MPS3704	5/1.00	2N4409	5/1.00
PN2222 Plastic	7/1.00	2N3705	5/1.00	2N5086	4/1.00
2N2369	5/1.00	MPS3705	5/1.00	2N5087	4/1.00
2N2369A	4/1.00	2N3706	5/1.00	2N5088	4/1.00
MPS2369	5/1.00	MPS3706	5/1.00	2N5089	4/1.00
2N2484	4/1.00	2N3707	5/1.00	2N5129	5/1.00
2N2906	4/1.00	2N3711	5/1.00	PN5134	5/1.00
2N2907	5/1.00	2N3724A	.65	PN5138	5/1.00
PN2907 Plastic	7/1.00	2N3725A	1.00	2N5139	5/1.00
2N2925	5/1.00	2N3772	2.25	2N5210	5/1.00
MJE2955	1.25	2N3823	1.00	2N5449	3/1.00
2N3053	2/1.00	2N3903	5/1.00	2N5951	3/1.00

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-99	100-		1-9	10-99	100-
10 pf	.05	.04	.03	.001µF	.05	.04	.035
22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075
100 VOLT MYLAR FILM CAPACITORS							
.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22
+20% DIPPED TANTALUMS (SOLID) CAPACITORS							
.1/35V	.28	.23	.17	1.5/35V	.30	.26	.21
.15/35V	.28	.23	.17	2.2/25V	.31	.27	.22
.22/35V	.28	.23	.17	3.3/25V	.31	.27	.22
.33/35V	.28	.23	.17	4.7/25V	.32	.28	.23
.47/35V	.28	.23	.17	6.8/25V	.36	.31	.25
.68/35V	.28	.23	.17	10/25V	.40	.35	.29
1.0/35V	.28	.23	.17	15/25V	.63	.50	.40
MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS							
Axial Lead				Radial Lead			
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.14	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

Circle 200 on inquiry card.

Circle 200 on inquiry card.

Structured Programming Macros for the 8080 and Z-80

Structured Analysis Systems has developed SP80, a set of structured programming macros for the 8080 and Z-80. Macro libraries are available for the TDL Z-80 assembler V2.2 and the Intel macro standard. SP80 is said to provide all common structured programming constructs such as: DO for count iteration, IF-ELSE for 2 path conditions, SELECT-CASE for multiple path branching, REPEAT-UNTIL and WHILE loop constructs as well as a special LOOP-EXITIF-ENDLOOP which allows multiple exits from embedded loops. All constructs allow signed and unsigned relational tests (EQ, NE, LE, LT, GE, GT) and condition code testing. Available with the TDL version is the use of conjunction (AND) and disjunction (OR) in any construct.

A manual containing listings of all macros in the two libraries; a discussion of macro syntax, constraints, memory and execution time requirements; a detailed example with corresponding conventional program, and general notes and suggestions is available for $19. A disk containing the macro libraries is available for $19 in CP/M file format. Contact Structured Analysis Systems, POB 2745, Reston VA 22091. ■

Circle 535 on inquiry card.

COSMAC 1802 Simulator

The COSMAC 1802 simulator program enables a 6502 processor to execute the COSMAC 1802 instruction set. The simulator does this by interpreting COSMAC instructions in a normal program sequence. All internal COSMAC registers are available for examination. They may be viewed statically in a single step mode or dynamically in a trace mode. All COSMAC software features are presently supported with the exception of direct memory access (DMA).

This simulator is now available in a KIM-1 version as a development and debugging tool for COSMAC software. It will run on a KIM-1 with no additional hardware or software required. In its minimum configuration the simulator leaves two full pages of memory open for COSMAC programs. It can be relocated in read only memory and can be readily adapted to other microcomputers using the 6502 processors.

The complete package contains a KIM-1 format cassette tape, user manual and a complete assembly level source and object listing. It is priced at $10 plus $1.50 for postage and handling. For further information write to Dann McCreary, 4758 Mansfield St, #2B, San Diego CA 92116. ■

Circle 537 on inquiry card.

Software for 8080 Processor

Micro Business software is designed to run on an 8080 processor with a FORTRAN compiler.

The general ledger (G/L) is designed for accountants and is generalized and flexible. There are over 20 programs in the system. It allows over 200 accounts with nine levels of totals, percentages on profit and loss capabilities. It forces balanced entry of transactions, verifies validity of accounts, and automatically puts income and expense totals in balance sheet form.

The payroll program (P/R) prints checks; calculates taxes; handles multipay periods, salaried and hourly employees, W2 forms, check register, department reporting, check numbers and more.

The G/L and P/R (object code) are priced at $775 each; A/R, and A/P are $495 each, or all four for $2250. The user's manual is $15 with credit towards purchase of software. For more information contact Engram Associates Inc, POB 9885, Little Rock AR 72219. ■

Circle 539 on inquiry card.

Software for CP/M Systems

Two related software products, Sort and File Index, which will operate on any size CP/M system, have been announced by Rothenberg Information Systems Inc, 260 Sheridan Av, Palo Alto CA 94306.

Sort will sort ASCII files in ascending or descending order. Short records are treated as if they contained blanks in the extended areas. The keys may be as long or short as desired and the multikey version permits up to 20 different keys.

File Index reads a series of floppy disks placed in the B drive and writes a copy of their directories onto the named file on drive A. This file may be listed or directly sorted with the sort program to produce an alphabetized list of files across all of the disks. A provision is made to prefix each directory entry with a disk name. If the disk has a file which has a second name of LBL, then File Index will use the first name as the disk name. If this file does not exist, the program will prompt the user for a name for the disk.

The Sort program is available in a single key version for $95; a multikey version is available for $145. The File Index program is available for $45 and requires either Sort program to produce the alphabetized list. Order information should include registered CP/M serial number. ■

Circle 536 on inquiry card.

System Software for the 8080, 8085 and Z-80 Microprocessors

A new system software for the 8080, 8085, and Z-80 processors has been announced by ComputerCo Inc, 5833 Dorchester Rd, Charleston SC 29405. Designed around North Star's BASIC version 6 with 14 digit precision, KFAM saves the user time in coding the original application program or modifying an existing subsystem.

The application programmer utilizes KFAM subroutines to handle data transmittal, packing and unpacking of data to maximize storage area, sorting upon input by keys, opening and closing of files, self-verifying of files, and the modular design of application software. KFAM contains a keyboard input utility for displaying data on a video screen, accepting the keyboard input, cursor positioning, and validation of data. Utilities to add records, delete records, and examine or alter existing records are included.

KFAM eliminates the need for sorting of input data by utilizing keys as new records are written to the files. The key allows for random access during batch processing.

The KFAM system software is available complete with documentation for $550. Documentation only without source code is $75. It is available on tape or disk. Application software is also available. ■

Circle 538 on inquiry card.

Screen Oriented Text Editor

Aox Associates announces MATE, a screen oriented text editor for 8080 or Z-80 microcomputers with floppy disks running under iCOM or TDL FDOS. MATE expands upon the capabilities of other text editors by dividing the screen into text display and command string sections. TECO-like command strings use iteration, conditional branching, and macros to operate on ten allocated buffers.

The independent text section of the screen instantly reflects any changes in the edit buffer, with text moving up and down or right and left as commands modify the buffer. In another mode, keystrokes are directly entered on the screen and in the text. MATE can be used with the VDM-1 or a similar video display board. Fast screen updates can also be obtained with a video terminal, since extensive display driver software utilizes the addressable cursor to make only necessary changes.

A wide variety of character, word, line and paragraph oriented commands are entered in the separately scrolling command section of the display. Command strings can range in complexity from a single character through full text editing programs.

MATE is available on an 8 inch floppy disk for $49.50, including 9 K bytes of object code for the editor, and object and source code for several screen, keyboard, and printer drivers. The user and interface manual (which can be purchased separately for $5, refundable with complete order), gives instructions to help adapt these drivers to other hardware. For further information contact Aox Associates, POB 558, Somerville MA 02143. ■

Circle 540 on inquiry card.

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IA Expands S-100 Line

Video Display Board

Featuring a full 128 upper/lower case ASCII character set stored in a 1K buffer memory. Easy to read 16 line x 64 character format can be displayed on an inexpensive video monitor or a **modified** TV set. Includes a TTY software driver. Add our powerful K 2 FDOS to create a versatile operator console.

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Power full disk software in the DEC tradition. Includes Text Editor (TED), File Package (PIP), Debugger (HDT), Assembler (ASMBLE), HEXBIN, 1 COPY, System Generator (SYSGEN). Command syntax follows Digitals OS-8, RT/11 format. First in a family of high level software. Soon to be released, FORTRAN & Pascal Compilers.

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Field-proven reliable engineering

Over 10,000 boards worldwide prove Ithaca Audio provides the quality and reliability you demand.

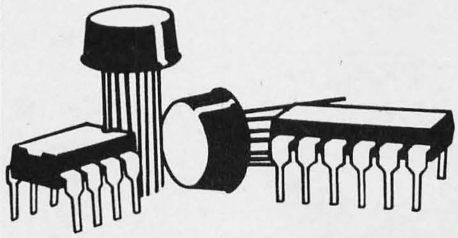
Ithaca Audio Boards are fully S-100 compatible, featuring gold edge connectors and plated-through holes. All boards (except the Protoboard) have fully buffered data and address lines, DIP switch addressing, solder mask and parts legend.

Z-80 CPU Board Most powerful 8 bit central processor available. Featuring power-on-jump, provision for on-board 2708. Accepts most 8080 software. **$35.00**

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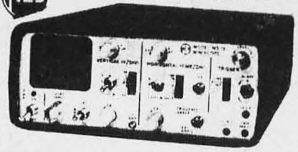
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- 15 megahertz bandwidth.
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MS-15 . . . . $318
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CSC



Model LP-1
Hand-held logic probe provides instant reading of logic levels for TTL,* DTL., HTL. or CMOS. **Input Impedance:** 100,000 ohms. **Minimum Detectable Pulse:** 50 ns. **Maximum Input Signal (Frequency):** 10 MHz. **Pulse Detector (LED):** High speed train or single event. **Pulse Memory:** Pulse or level transition detected and stored.
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High speed logic probe. Captures pulses as short as 10 ns. **Input Impedance:** 500,000 ohms. **Minimum Detectable Pulse:** 10 ns. **Maximum Input Signal (Frequency):** 50 MHz. **Pulse Detector (LED):** High speed train or single event. **Pulse Memory:** Pulse or level transition detected and stored.
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Exact replacement for Shugart 801R
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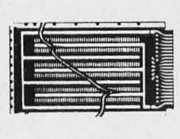
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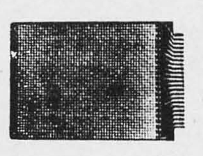
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Universal Microcomputer/processor plugboard. Use with S-100 bus. Complete with heat sink & hardware. 5.3" x 10" x 1/16".

8801-1

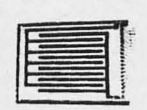
Same as 8800V except plain; less power buses & heat sink.

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PROM S

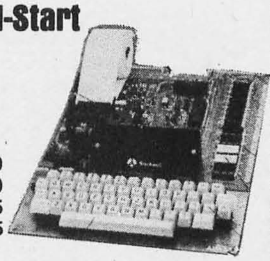
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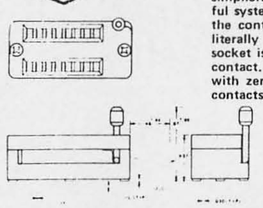
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16K	$199.00
24K	$249.00
32K	$299.00

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EPROM BOARD KITS

EPM-1 (uses up to 4K of 1702)	$59.95
JG8/16 (uses 2708 or 2716)	$69.95

STATIC RAM BOARDS

JADE 8K

Kits:	450ns	$125.95
	250ns	$149.75
Assembled & Tested:		
	450ns	$139.75
	250ns	$169.75
Bare Board:		$ 25.00

16K – Uses 2114's (low power)
Assembled & Tested:

RAM 16	(250ns)	$375.00
RAM 16B	(450ns)	$325.00

16K with memory management
Assembled and Tested:

RAM 65	(250ns)	$390.00
RAM 65B	(450ns)	$350.00

32K Static
Assembled & Tested:

250ns	$795.00
450ns	$725.00
250ns Kit	$575.00

JADE Computer Products

4901 W. ROSECRANS AVENUE
Department "B"
HAWTHORNE, CALIF. 90250
U.S.A.

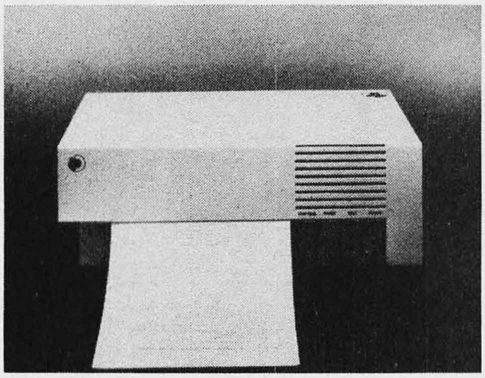
Telephone: (213) 679-3313
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Cash, checks, money orders, and credit cards accepted. Add freight charge of $2.50 for orders under 10 lbs. and $1.00 service charge for orders under $10.00. Add 6% sales tax on all parts delivered in California. Discounts available at OEM quantities.

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Circle 195 on inquiry card.

Versatile Impact Printer



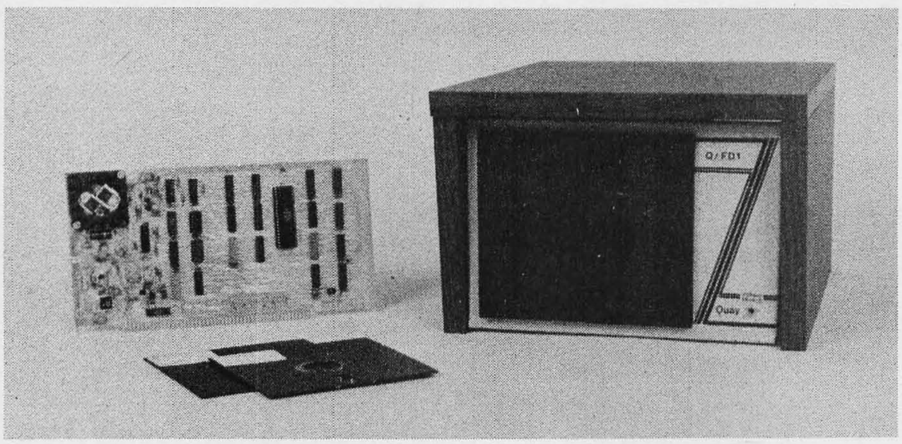
The Integral IP-125 impact printer features an RS-232C serial interface, parallel transistor-transistor logic level interface and full upper and lower case ASCII character set (96 characters) as standard equipment. Capable of printing multiple copies on 8.5 inch (21.59 cm) roll, fanfold or sheet paper, the processor-controlled IP-125 incorporates a 256 character multiline buffer to achieve an instantaneous print rate up to 100 characters per second, with a sustained throughput of 50 characters per second at 80 columns per line.

The printer has few moving parts and features a re-inking ribbon. The unit measures 17.25 by 7 by 11.5 inches (43.82 by 17.78 by 29.21 cm). Line length is 80 columns at 10 columns per inch (7 by 7 dot matrix format), with line lengths to 132 columns, print rates to 165 characters per second, print densities of 8.3, 10, 12 and 16.5 characters per inch and a full video screen size multiline buffer (2048 characters) optional. Serial transmission rates of 110 to 1200 bps are switch selectable.

The Integral IP-125 impact printer sells for $799. Literature is available from Integral Data Systems Inc, 5 Bridge St, Watertown MA 02172.■

Circle 579 on inquiry card.

S-100 Floppy Disk System



A floppy disk system for use in S-100 bus computers is available from Quay Corp, POB 386, Freehold NJ 07728. The Quay 80 F1 system includes the Q/80 FDC floppy disk controller board (capable of supporting up to four disks); QDOS disk based operating system; the Q/FD1 125 KB 5¼ inch band driven disk drive with power regulator and interface cable; and the Q/80 FC floppy disk cabinet. In addition to the floppy disk support, the Q/FDC has available a programmable 8 bit, transistor-transistor logic compatible parallel input and output (IO) port capable of supporting standard peripheral devices such as line printers, tape punches, keyboards, etc.

The Quay 80 F1 system is priced at $795. The add-on drive (Q/FD1) is priced at $395.■

Circle 580 on inquiry card.

Video Monitor and Receiver

The new model VMR-120 is a 12 inch (30 cm) diagonal monochrome video monitor and receiver. It is suited for industrial, security, studio or computer display applications, with separate UHF connections for video in and thru; RCA connector for audio in, and a termination switch. The VMR-120 is also available as a monitor only. Model VMR-120A has the additional feature of an 8 pin video tape recorder (VTR) connector, separate UHF and RCA connectors for TV video, and audio out for off the air recording. Power requirements are 117 V 60 Hz 30 W, or 12 to 16 VDC, 14 W. Weight is 16 pounds (7.26 kg) and the units are equipped with a carrying handle. The prices are $199 for the VMR-120 and $215 for the VMR-120A. A 19 inch (48 cm) monochrome receiver and monitor is available for $350. For further information contact Video Marketing Inc, 328 Maple Av, Horsham PA 19044.■

Circle 583 on inquiry card.

Bus Addressable Numeric Display



The Pichler DP08 is an 8 digit bus-addressable panel display with its address encoded in the bus connector to facilitate interchanging or replacement without internal adjustment or rewiring. This permits virtually unlimited system configurations. Binary weighted address select lines allow up to 32 of the peripheral interface adapter compatible displays to operate from the same 9 wire signal bus. Once addressed the display accepts up to eight binary coded decimal encoded digits from the bus at 200 K byte digits per second and stores them in a programmable memory for subsequent display. While accessing the programmable memory, the unit automatically blanks.

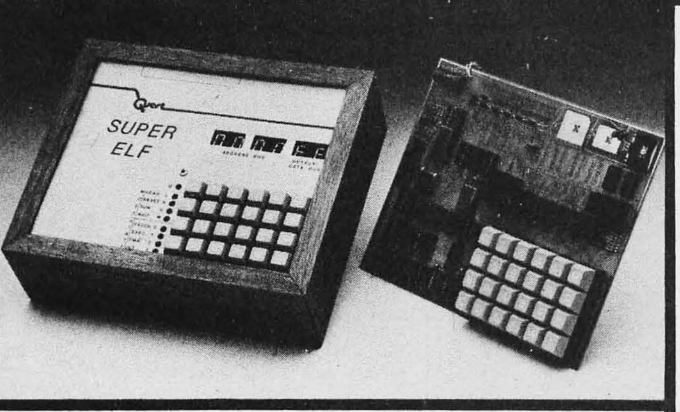
Available in table top and front and rear panel mount versions, the DP08 measures 5 by 2 by 6 inches (12.7 by 5.08 by 15.25 cm). Both can be supplied with an optional integral thumbwheel for address selection. The DP08 is priced from $215 depending on configuration. Contact Pichler Associates, 410 Great Rd, Littleton MA 01460.■

Circle 581 on inquiry card.

Hard Disk for All Popular Microcomputer Based Systems

The EXCOMP DCF10 disk controller provides an interface for fixed and removable disk media. Using industry standard 3, 6, and 12 M byte disk drives, the DCF10 can control and format up to four drives for a total formatted storage capacity of 40 M bytes. The disk drives may use an IBM 2315 or 5440 removable cartridge and up to three fixed platters. The DCF10 may also be used with fixed only disk drives. A universal 8 bit processor interface permits the controller to be used with popular microcomputer based systems. Due to the high data rates involved, the controller should be connected to the processor through either a direct memory access or buffer storage system. The DCF10 is priced at $2100 in quantities of 1 to 4. For further information contact XComp Inc, 9915-A Business Park Av, San Diego CA 92131.■

Circle 582 on inquiry card.



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Quest ELECTRONICS

QUEST Cosmac Super Elf Computer $106.95

Compare features before you decide to buy any other computer. There is no other computer on the market today that has all the desirable benefits of the **Super Elf** for so little money. The Super Elf is a small single board computer that does many **big** things. It is an excellent computer for training and for learning programming with its machine language and yet it is easily **expanded with additional memory, Tiny Basic, ASCII Keyboards, video character generation, etc.**

The **Super Elf** includes a **ROM** monitor for program loading, editing and execution with **SINGLE STEP for program debugging** which is not included in others at the same price. With **SINGLE STEP** you can see the microprocessor chip operating with the **unique Quest** address and data bus displays **before, during** and **after** executing instructions. Also, CPU mode and instruction cycle are shown on several LED indicator lamps.

An RCA 1861 **video graphics** chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a **speaker system** included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

A 24 key **HEX keyboard** includes 16 HEX keys plus **load, reset, run, input, memory protect, memory select, monitor select** and **single step**. Large, on board displays provide output and optional **high and low address**. There is a 44 pin standard connector for PC cards and a 50 pin connector for the **Quest Super Expansion Board**. Power supply and sockets for **all** IC's are included in the price plus a detailed 90 page instruction manual.

Many schools and universities are using the Super Elf as a course of study. OEM's use it for training and research and development.

Remember, other computers only offer Super Elf features at additional cost or not at all. **Compare before you buy. Super Elf Kit $106.95, High address option $8.95, Low address option $9.95. Custom Hardwood Cabinet** with drilled and labelled front panel **$24.95. NiCad Battery Backup Kit $4.95.** All kits and options also come completely assembled and tested.

Questdata, a 12 page monthly software publication for 1802 computer users is available by subscription for $12.00 per year. New 100 page software manual Vol.1 $4.95.

Tiny Basic for ANY 1802 System

Cassette $10.00. On ROM Monitor $38.00. Super Elf owners, 30% off. **Object code listing or paper tape with manual $5.50. Original ELF Kit Board $14.95.**

Super Expansion Board with Cassette Interface $89.95

This is truly an astounding value! This board has been designed to allow **you** to decide how you want it optioned. **The Super Expansion Board comes with 4K of low power RAM** fully addressable anywhere in 64K with built-in memory protect and a **cassette interface**. Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the **Super Elf**. The board includes slots for up to 6K of **EPROM** (2708, 2758, 2716 or TI 2716) and is **fully socketed** ($12.00 value). EPROM can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/editor and error checking multi file cassette read/write software, (relocatible cassette file) another exclusive from Quest. It includes register save and readout, block move capability, and video graphics driver with blinking cursor. The Super Monitor is written with subroutines allowing users to take advantage of monitor functions simply by calling them up. Improvements and revisions are easily done with the monitor. If you have the **Super Expansion Board** and **Super Monitor** the monitor is up and running at the push of a button.

Other on board options include **Parallel Input and Output Ports with full handshake.** They allow easy connection of an ASCII keyboard to the input port. **RS 232 and 20 ma Current Loop** for teletype or other device are on board and if you need more memory there are two **S-100** slots for static RAM or video boards. A Godbout 8K RAM board is available for $135.00. **Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50.** A **50 pin connector set** with ribbon cable is available at $12.50 for easy connection between the **Super Elf** and the **Super Expansion Board.**

The **Power Supply** for the Super Expansion Board is a 5 amp supply with + 8v ± 18v + 12v − 5v. Regulated voltages are ±5v & +12v $29.95. −12 volt optional. Deluxe version includes the case at $39.95.

INTEGRATED CIRCUITS

7400TTL	
7400N	.17
7402N	.17
7404N	.19
7409N	.23
7410N	.17
7414N	.63
7420N	.17
7422N	1.39
7430N	.20
7442N	.50
7445N	.69
7447N	.60
7448N	.69
7450N	.17
7474N	.29
7475N	.49
7485N	.88
7489N	2.00
7490N	.43
7492N	.43
7493N	.43
7495N	.69
74100N	.90
74107N	.29
74121N	.34
74123N	.59
74125N	.39
74145N	.69
74150N	.95
74151N	.69
74154N	1.00
74157N	.69
74161N	.87
74162N	.87
74163N	.87
74174N	.96
74175N	.90
74190N	1.15
74192N	.87
74193N	.85
74221N	1.55
74298N	1.65
74365N	.66
74366N	.66
74367N	.66

74LS00 TTL	
74LS00N	.25
74LS02N	.25
74LS04N	.25
74LS05N	.25
74LS08N	.25
74LS10N	.25
74LS13N	.40
74LS14N	.90
74LS20N	.25
74LS22N	.25
74LS28N	.41
74LS30N	.25
74LS33N	.39
74LS38N	.30
74LS74N	.35
74LS75N	.47
74LS90N	.51
74LS93N	.51
74LS95N	1.89
74LS107N	.35
74LS112N	.35
74LS113N	.35
74LS132N	.72
74LS136N	.35
74LS151N	.67
74LS155N	.67
74LS157N	.67
74LS162N	.91
74LS163N	.91
74LS174N	.95
74LS190N	1.06
74LS221N	1.95
74LS258N	.67
74LS367N	.89

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CA3046	.67
CA3081	1.80
CA3082	1.90
CA3089	2.95
LM301AN/AH	.35
LM305H	.87
LM307N	.35
LM308N	.89
LM309H	1.15
LM309K	.95
LM311H/N	.90
LM317T/K	2.92
LM318	1.35
LM320K-5	1.20
LM323K-5	6.95
LM320K-12	1.35
LM320K-15	1.35
LM320T-5	1.60
LM320T-8	1.60
LM320T-12	1.50
LM320T-15	1.60
LM324N	1.15
LM339N	1.55
LM340K-5	1.10
LM340K-8	1.10
LM340K-12	1.10
LM340K-15	1.10
LM340K-24	1.10
LM340T-5	1.10
LM340T-8	1.10
LM340T-12	1.10
LM340T-15	1.10
LM340T-18	1.10
LM340T-24	1.10
LM343H	4.50
LM370	1.15
LM377	4.50
LM379	5.00
LM380N	1.00
LM381	1.60
LM382	1.60
LM703H	.40
LM709H	.28
LM723H/N	.50
LM733N	.67
LM741CH	.35
LM741N	.25
LM747H/N	.62
LM748N	.35
LM1303N	.82
LM1304	1.10
LM1305	1.27
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LM1310	2.75
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LM3905	1.75
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NE540L	2.89
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NE555V	.43
NE556A	.79
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NE566V	1.50
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78L08	.60
79L05	.70
78M05	.85
75108	1.75
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CD4006	1.10
CD4007	.21
CD4008	.21
CD4009	.39
CD4010	.39
CD4011	.21
CD4012	.21
CD4013	.36
CD4014	.86
CD4015	.86
CD4016	.36
CD4017	.94
CD4018	.94
CD4019	.21
CD4020	1.02
CD4021	1.02
CD4022	.86
CD4023	.21
CD4024	.75
CD4025	.21
CD4026	1.51
CD4027	.36
CD4028	.79
CD4029	1.02
CD4030	.21
CD4035	1.02
CD4040	1.02
CD4042	.71
CD4043	.63
CD4044	.63
CD4046	1.67
CD4049	.36
CD4050	.36
CD4051	1.13
CD4060	1.42
CD4066	.71
CD4068	.40
CD4069	.40
CD4070	.40
CD4071	.21
CD4072	.21
CD4073	.21
CD4075	.21
CD4076	1.75
CD4078	.40
CD4081	.21
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CD4508	4.25
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CD4511	.94
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CD4516	1.10
CD4518	1.02
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74C90	1.15
74C93	1.40
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Solder Tin Low Profile

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8	.15	22	.30
14	.18	24	.35
16	.20	28	.42
18	.27	36	.58
20	.29	40	.57

3 level wire wrap gold.
14 pin .25 16 pin .27
2 level 14 pin ww .20

WIRE WRAP LEVEL 3

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16	.27	28	1.00
18	.57	40	1.23

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2N2907A	.25
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2N3638	.25
2N3643	.25
2N3904	.18
2N3906	.18
2N3055	.69
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100 per type .015 5 per type 6.75

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Cliplite LED Mounting Clips	8/$1.25

(specify red, amber, green, yellow, clear)

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Batt. oper. General purpose or medical 32°–230°F. Disposable probe cover ±.2° accuracy. Comp. Assy. in compact case. Switches from F° to C°.

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4K EPROM Kit	114.95
I/O Board Kit	44.50
Extender Board w/connector	12.50
Video Interface board kit	125.00
16K EPROM board kit w/o PROMS	74.50
16K Static RAM board kit	395.00
North Star Floppy Disk Kit	$665.00
Additional Drive Kit	415.00

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MM5865 Stopwatch Timer	9.00
PC board	7.50
Switches Mom. Pushbutton	.27
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3 Digit Universal Counter Board Kit Operates 5–18 Volt DC to 5 MHz typ. .125" LED display	**10.50**
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10V 1.2 amp wall plug	4.85
12V 6 amp	12.95

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MAN1	CA	.270	2.90
MAN3	CC	.125	.39
MAN72/74	CA/CA	.300	1.00
DL704	CC	.300	1.25
DL707/DL707R	CA	.300	1.00
DL727/728	CA/CC	.500	1.90
DL747/750	CA/CC	.600	1.95
DL750	CC	.600	1.95
FND359	CC	.357	.70
FND500/507	CC/CA	.500	1.35
FND503/510	CC/CA	.500	.90
FND800/807	CC/CA	.800	2.20
3 digit Bubble			.60
4 digit bubble			.80
DG8 Fluorescent			1.75
DG10 Fluorescent			1.75
5 digit 14 pin display			1.00
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7520 Clairex photocells			.39
TIL311 Hex			9.50

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3200		50V	2.50
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5800		40V	3.00
6100		40V	3.00
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82000		15V	6.00
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DC clock with 4-.50" displays. Uses National MA-1012 module with alarm option. Includes light dimmer, crystal timebase PC boards. Fully regulated, comp. instructs. Add $3.95 for beautiful dark gray case. Best value anywhere.

RCA Cosmac VIP Kit $229.00

Video computer with games and graphics. Fully assem. and test. **$249.00**

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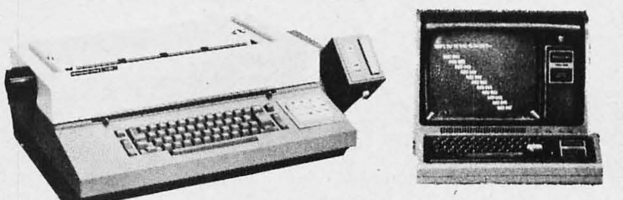
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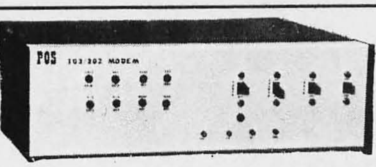
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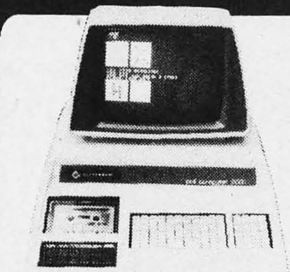
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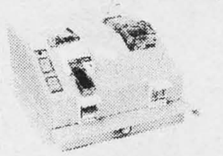
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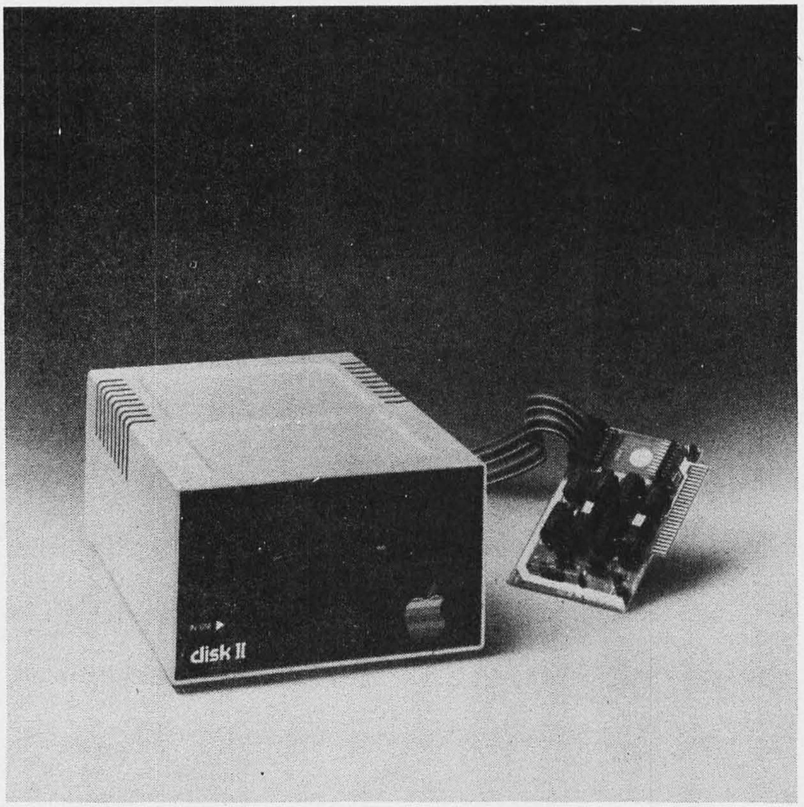
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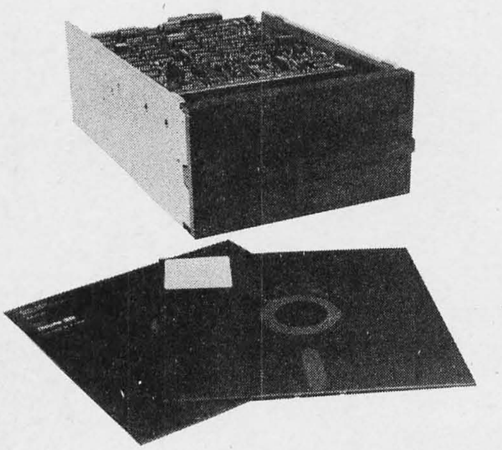
The Apple II disk drive is available from Apple Computer Inc, 10260 Bandley Dr, Cupertino CA 95014. Disk II's rapid access to programs and data makes possible a wide variety of new applications including personal finance, small business systems, home record keeping and many more.

Disk II's disk operating system (DOS) software provides dynamic disk space allocation so a system user need not be concerned with the size or physical location of a file on a disk. The DOS performs this housekeeping function; the user simply indicates the name of the file being stored or retrieved. The DOS provides compatibility with existing languages through the use of standard BASIC commands.

The Disk II subsystem consists of an intelligent interface card and either one or two minifloppy drives. The computer will handle up to seven controller cards and 14 drives for instant access to more than 1.6 million bytes of data. The combination of a bootstrap loader in read only memory and an operating system in programmable memory provides powerful disk handling capability with the following features: full disk capability for systems with as little as 16 K bytes of programmable memory, the ability to load and store files by name, random and sequential access, automatically generated file name directories, storage capacity of 116 K bytes per disk, and the ability to be driven from Apple II power supply with no other power required. The Disk II is priced at $495.■

Circle 556 on inquiry card.

Dual-Sided Floppy Disk Drive Compatible with IBM Disk 2 and 2D



This new 8 inch, dual-sided floppy disk drive is capable of recording and reading data on both sides of an IBM (or equivalent) disk 2 or 2D. The drive, designated FD650, offers an immediately addressable unformatted storage capacity of 1.6 M bytes.

The FD650 is capable of double density operation using modified frequency modulation encoding. All electronics are on a single printed circuit board. Track to track access time is three ms, with head load time of 35 ms, and track settling time of 15 ms. The user can daisy chain up to eight drives.

Head positioning is achieved by a steel band attached to the head carriage and to a drive pulley on the shaft of a 4 phase 1.8° permanent magnet stepper motor. Each step of the motor causes the head to move one track.

The FD650 is priced at $755 in single quantities. Contact Pertec Computer Corp, 9600 Irondale Av, Chatsworth CA 91311.■

Circle 557 on inquiry card.

Where Do New Product Items Come From?

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Modular Minifloppy Storage System

Designated the Diskwriter SA-11, this modular minifloppy storage system allows the user to field upgrade to a dual drive and/or add memory for programmability.

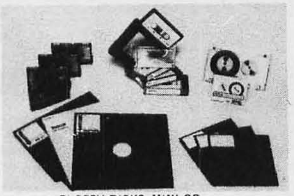
The normal operating software such as insert, delete, selective print, split data rate, global find or replace, columnar insert, etc, are included. The software allows the user, as an extra option, to set up prompts from the keyboard or from a disk. Any dumb terminal can be upgraded to intelligent terminal capability.

The price of the Diskwriter SA-11 is $1495. For further information, contact Hands On Terminals Inc, 1215 S E Ivon, Portland OR 97202.■

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Circle 100 on inquiry card.

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3rd PRIZE- AUDIO INTERFACE OR $200 CASH

M	I	C	R	O	16	
O	N	L	A	P	11	
O	L	I	V	E	14	= 61
N	E	V	E	N	9	
S	T	E	D	S	11	

WHY CAN THE HUMAN MIND SOLVE THIS PUZZLE EASIER THAN THE MACHINE MIND? SOMEWHERE ON EARTH THERE MUST BE A COMPUTER THAT CAN BEAT THE HUMANS WHO ENTER THIS CONTEST. THIS IS A TOTALLY OBJECTIVE PUZZLE. PERFECT FOR COMPUTER SOLUTION. WINNERS ARE DETERMINED SOLELY ON THEIR ABILITY TO GET THE HIGHEST SCORE IN ABOUT 1 MONTHS TIME. 4th & 5th PRIZE ARE NOW $100.

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CATCH-A-PULSE II LOGIC PROBE



- 10 Nsec pulse response
- Open circuit detection
- Replaceable tip & cord
- High input impedance
- Pulse stretching
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10 Nsec SPEED AT 4 to 15V LEVELS ONLY $44.95

Compatible with DTL, TTL, CMOS, MOS and Microprocessors using a 4 V to 15 V power supply. Thresholds automatically programmed for multi logic family operation. Automatic resetting memory for single or multi pulse detection. No adjustment required. Visual indication of logic levels, using LEDs to show high, low, bad level or open circuit logic and pulses. Highly sophisticated, shirt pocket portable (protective cap over tip and removable coiled cord). Eliminates need for heavy test equipment. A definite plus in time and money for engineer and technician.

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Monitors * Combination Rcvr/monitor sets * Modulator kits * B-W Cameras * Color Cameras * Audio Subcarrier kits * Parts



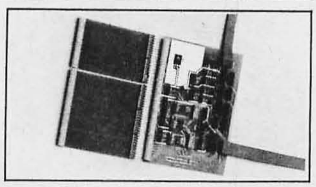
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6800 OWNERS

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Extend both the 30 and 50 pin buses in SWTP 6800. **Both for $19.95.**

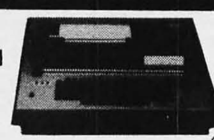
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ASCII  ASCII

IBM SELECTRIC® BASED I/O TERMINAL WITH ASCII CONVERSION INSTALLED $645.00

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cost effective
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$735 plus shipping

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- All 128 ASCII Codes
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- 24 Lines; 12 inch Screen
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- Self Diagnostic Test

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Quiet Buss™
$29.95
8803-18
18 slot
IMSAI

The Quiet Buss from California Industrial is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy FR-4 epoxy glass.

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Even if we have to give them away, we're going to ship more 43's in 1979 than the aggregate of all our competitors.

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$925.	875.	850.	825.

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Shugart Associates

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The most cost effective way to store data processing information, when random recall is a prime factor. The SA800 is fully compatible with the IBM 3740 format. Write protect circuitry, low maintenance & Shugart quality.

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Qty.	fe.	male	hd.
10	3.45	2.45	1.15
25	3.15	2.25	1.05
100	2.85	1.90	.95
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1K	1.97	1.37	.73

Edge Connectors

GOLD
100 PIN
IMSAI/ALTAIR

Imsai solder .125x.250	$4.95	3/$10.00
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25/50 solder tab .156"	$1.09	3/$2.00
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SPERRY UNIVAC KEYBOARD



$24.88

The famous Sperry Univac 1710 Hollerith keyboard assembly is now available from California Industrial for only $24.88. The ideal computer input device for accountants and mathematicians. The numeric keys are placed on the lower three rows to resemble a ten key adding machine. This format allows one handed numeric data entry.
Original cost was $385. Used but guaranteed in excellent condition. Complete with documentation.

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$13.95

The Atari R.F. Modulator allows computer data to be displayed directly upon your existing television system. This unit converts the signal from the Apple II and other video sources into television frequencies. Operates from single 5 volt supply. Complete with metal case, mating R.F. connector and 15 feet of coax cable. Schematics and instructions included.

Assembled

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APPLE II 16K MEMORY

COLOR • GRAPHICS • SOUND
$1024 PLUS SHIPPING
Mfg. Sug. Retail.... $1195

Scotch® BRAND

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Won't drop a BIT!
$5.50

DISKETTES
8 inch Soft (IBM)
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APPLE RS-232

Serial Interface $59.95
Interfaces Apple II to Teletype or other serial printer.
ELECTRONIC SYSTEMS

® dataphone model 2400 $249.

Factory new Bell System modems. Some units show cosmetic damage. Documentation not included. Other models available call for price and quantities.

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Mullen $34.95

Facilitates design and troubleshooting of all S-100 microsystems. Includes logic probe along with high-low and pulse LED display.
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GP100-Maximum design versatility along with standard address decoding and buffering for S100 systems. Room for 32 uncommitted 16 pin IC's, 5 bus buffer & decoding chips, 1 DIP address select switch, a 5 volt regulator and more.
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TRS-80 APPLE II $65
16k memory (8) 4116's

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To obtain the best pricing on memory we have made volume commitments to our suppliers, which in turn affords us the opportunity to sell these circuits at the most competitive prices. Please contact us if you if you have a demand for volume state of the art memory products.

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2114 1Kx4 450	6.95	6.50	6.25	6.00	5.75
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4044 4Kx1 250	9.95	9.50	9.00	*	*
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5257 low pow.	7.95	7.50	7.05	6.75	6.45

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CLARE-PENDAR General Instrument Corp. KEYBOARD ASCII ENCODED



This is a one time purchase of NEW Surplus keyboards, recently aquired from the Telecommunications Division of the Singer Corporation.
The keyboard features 128 ASCII characters in a 63 key format, MOS encoder circuitry "N" key rollover, lighted shift lock, control, escape and repete functions.
Sloped pannel and positive feel switches, makes this professional quality keyboard an excellent buy at only $64.95.
Limited Quantities.

63 KEY **$64.95**

Thumbwheel switch

Ten position BCD
$1.39 ea.

10	50
$1.19	.89

MINIATURE SWITCHES

your choice

	10	50	100	1k
$.98	$.88	.81	.73	.66

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7101 C&K	ON-NONE-ON
7107 jbt	ON-OFF (mnt. ON)
7108 CK	ON-(moment. ON)
Rocker JBT	DPDT
Rotary	3P-4-Pos.
Rotary	3P-6-Pos.
Push B (N.O.)	$.39 ea. 4/$1

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ELECTROLYTICS

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80,000/10v.	3.95	3.49	2.95
4500/50v.	$1.49	1.35	1.19
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.1 disc	$.12	.09	.07
.01 disc	.06	.05	.04

50 Conductor RIBBON WIRE

$.69 Ft.
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6 vdc, 140mA	$1.39
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9 vdc, 200mA.	1.19
10 vAc, 300mA.	1.95

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Only 10,000 Available
NE555H
Leads fan out to fit Mini-DIP socket.
3 for $.98
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DIP Switch

$1.49 ea.

10	25	100	1K
$1.29	1.15	.97	.83

specify 7 or 8 pos.
SPST

Transistors

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2N3055	.69	.65	.59	.55
MJ3055	.79	.75	.69	.65
2N3772	1.59	1.49	1.39	1.29
2N3904	.15	.11	.09	.07
2N3906	.15	.11	.09	.07

Diodes

		10	25	100
1N4002	100v.	.08	06	.05
1N4005	600v.	.10	.08	.07
1N4148	signal	.07	.05	.04

jumbo red LED's

ea.	10	25	100
$.15	.13	.11	.09

TRANSFORMER

$.98
Output: 12v.ct. 175mA.
TRANSFORMER

9 foot

$1.49
Heavy duty grounded power cord and mating chassis connectors.

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2K 5K 10K 50K
5 for $.98

20	50	100
16¢	14¢	12¢

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900 Assorted Lengths
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250' Bulk Wire

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50ft. $.98
KYNAR WIRE WRAP

500	1,000	11,000
$9.	$15.	$105.

Battery wire wrapping tool
$34.95
$29.95 BW630

OK HOBBY WRAP-30 wire wrap & strip tool
$5.45

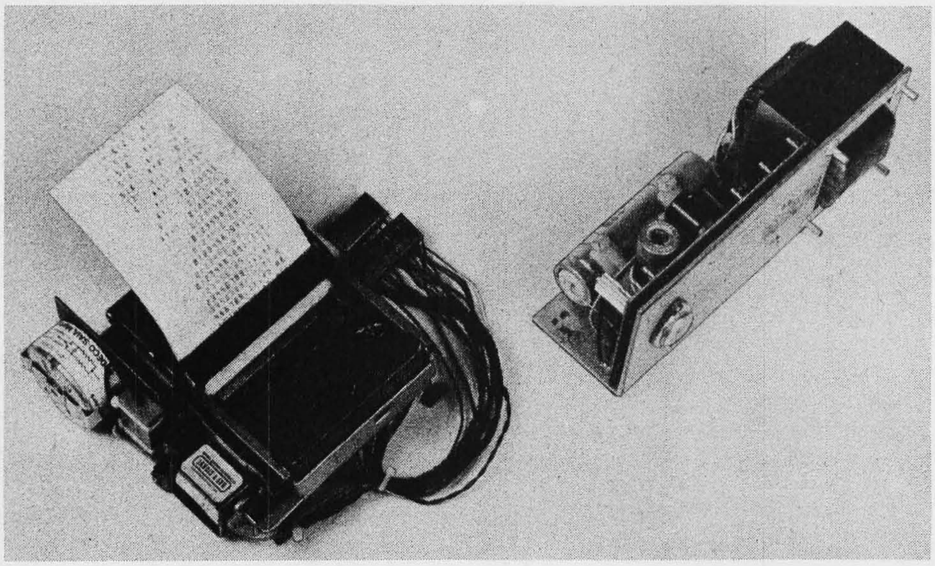
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Circle 39 on inquiry card.

Low Cost Impact Printing System



A family of impact print mechanisms, the associated controls, and power supplies for inexpensive column printing have been announced by Sodeco, 4 Westchester Plz, Elmsford NY 10523. Series PR15 and PR21 printing mechanisms can print either 15 or 21 columns, respectively, numeric only or full alphanumeric data. The printing is done at speeds of up to three lines per second for numeric models, or 15 lines per second for full alphanumeric. Measuring 5.8 by 6 by 2.3 inches (14.73 by 15.24 by 5.84 cm), the PR series printers use snap-in 2 color ribbon cartridges. The second color permits the highlighting of more important data or messages. Quantities of 100 or more are $105 for the 15 column printer and $130 for the 21 column model.

Sodeco also offers two interface/controllers. Model 4-621-9205 uses a F8 microprocessor while Model 4-621-9210 uses a Mostek 3870 processor. Both interfaces accept ASCII serial and 8 bit parallel, RS232C or BCD parallel data formats. Both interfaces contain all the circuitry required to operate the printers, including the hammer solenoid drivers, read only memory character generator, a full line buffer, timing control, full handshaking facilities and related logic necessary for interfacing and controlling the series PR printer. Prices for the 3870 based interface board are $120 and $250 for the F8 based board. In addition, the 3870 integrated circuit, completely programmed, is available separately for $40.

To provide power for the above system, Sodeco offers a custom power supply that has all the voltages required by the Series PR15 and 21 column printers and the associated interfaces. Designated the Model CP242, the unit is 2 3/4 by 3¼ by 7 3/4 inches (6.99 by 8.26 by 19.69 cm) and can operate either on 120 VAC, 60 Hz or 220 VAC, 50 Hz line. The CP242 is priced at $90.■

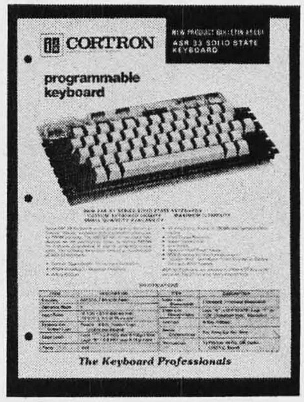
Circle 599 on inquiry card.

Keyboard Provides ASR 37 Teletype Format

The 77 key Model L69601 provides the ASR 37 Teletype format with all 128 ASCII characters and a high speed numeric entry pad, five cursor control keys and four spare key positions for custom use. This keyboard features 77 capacitive, low profile solderless key switches, double shot molded keytops, lighted Teletype lock, and two key rollover. The keyswitches offer the standard travel and force of the electric typewriter. This OEM keyboard is available assembled and tested for $139. For further information, contact Yestronics, POB 1892, S Hackensack NJ 07602.■

Circle 600 on inquiry card.

New Programmable Keyboard

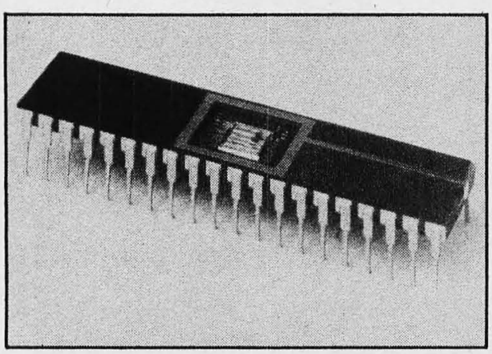


This standard ASR 33 keyboard is solid state and offers maximum flexibility due to programmable read only memory encoding. The ASR 33 can be purchased fully encoded or without programmable read only memory for customer programming to provide completely unique codes. Some of the standard features include N key rollover, working life in excess of 100,000,000 operation per keystation, MOS scanning and interlock generation. For additional information request Product Bulletin #K5001 from Cortron Division, Illinois Tool Works Inc, 6601 W Irving Park Rd, Chicago IL 60634.■

Circle 601 on inquiry card.

Synchronous Data Link Controller Circuit

This MOS/LSI programmable synchronous data link controller (SDLC)



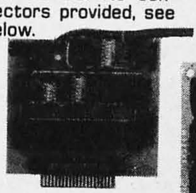
integrated circuit has been introduced by Western Digital Corp, 3128 Red Hill Av, Newport Beach CA 92663. This new device, the SD 1933A/B, has an NRZI encode and decode option and digital phase lock loop when in 32X mode. Fully compatible with IBM, HDLC, and ADCCP specifications, the SD 1933 controller interfaces parallel digital systems to synchronous serial data communication channels employing ADLC line protocol. In applications such as telecommunications, switching networks, packet switching, or in mainframe terminal communications, the SD 1933 replaces nearly 70 logic integrated circuits currently required for the same function.

Featuring synchronous full duplex operation, programmable modem control interrupts, error detection, and go ahead option for loop applications, the 40 pin chip is able to support bps rates to 1.5 MHz. Its 8 bit architecture enables it to provide a full set of modem controls. The SDLC controller may be used with all types of mainframe, minicomputer and microcomputer data buses. The protocol includes zero insertion and deletion, CRC generation and checking and automatic detection and generation of special control characters. A direct memory access mode is available. Double buffering of data enables the receiver buffer to hold data and status information while the transmitter buffer contains data and control information.■

Circle 602 on inquiry card.

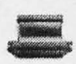
TRS-80 SERIAL I/O E.S.

• RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line. Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010C. No connectors provided, see below.





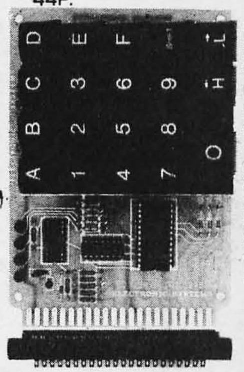
EIA/RS-232 connector Part No. DB25P $6.00, with 8'. 8 conductor cable $10.95 Part No. DB25P9.



3' ribbon cable with attached connectors to fit TRS-80 and our serial board $19.95 Part No. 3CAB40.

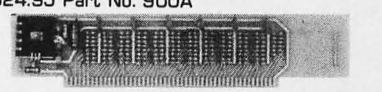
HEX ENCODED KEYBOARD E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX-3A. 44 pin edge connector $4.00 Part No. 44P.



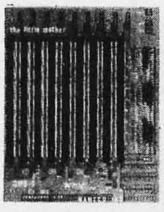
S-100 BUS ACTIVE TERMINATOR *

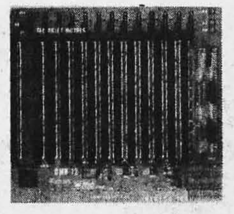
Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A



9 AND 13 SLOT MOTHER BOARDS WMC/inc.

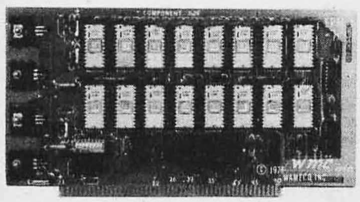
All traces are reflow solder covered and both sides are solder masked. The connectors used on these boards are the IMSAI™ type (.125" between pins, .250" between rows). Spacing between connectors is .750". All lines, except power and ground, have a passive RC network termination available. There is a kluge area available that will accept two 40 pin sockets and one 36 pin socket. The circuitry for supplying three separate regulated voltages to the kluge area is contained on the board. Part No. QMB-12 $40 bare, $105 kit, $120 assembled. Part No. QMB-9 $35 bare, $90 kit, $105 assembled.





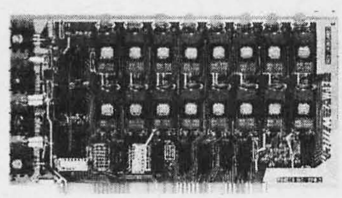
4K EPROM WMC/inc.

This board is designed to operate with any speed or power 1702A. Addressable in 4K byte increments and can be configured to occupy either 2K or 4K segments. It can be populated one memory chip at a time. Bare board $30, board with parts $200, assembled $230. Part No. EPM-1



16K OR 32K EPROM WMC/inc.

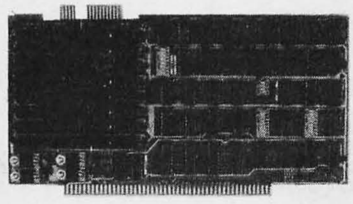
Designed to operate with any speed or power 2708 or single voltage (+5V) 2716. Addressable in 4K increments and can occupy multiples of 4K. It can be populated one memory chip at a time. Has bank addressing and Phantom Disable. The board comes with an exclusive software program that can be placed in a 2708 or 2716 that will, when used in conjunction with a RAM memory board, check out every line on the EPM-2. Bare board $30, board with parts with 2708 $455, assembled $485. Board with parts with 2716 $1,225, assembled $1,255. Part No. EPM-2



PIICEON

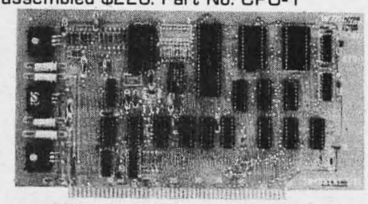
65K DYNAMIC RAM

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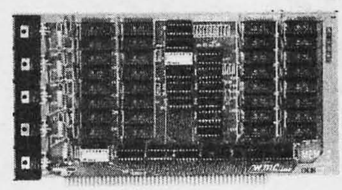
8080A CPU (With Eight Level Victor Interrupt Capability) WMC/inc.

Uses the 8080A and the 8224 clock chip. The crystal frequency used is 18 MHz and the vector interrupt chip is the 8214. The board will function normally without the interrupt circuitry. When the interrupt circuitry is built up, the board will respond to eight levels of interrupts. Designed to be a plug-in replacement for the IMSAI CPU board and will work in other computers with the appropriate modifications made to the ribbon cable connector pin out from the front panel. The board will work in systems without a front panel if the system has a PROM board that simulates the functions of the front panel. Bare board $30, with parts $185, assembled $220. Part No. CPU-1



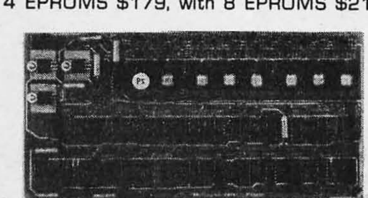
16K STATIC RAM WMC/inc.

Operates with any speed or power 2114. All input and output lines are fully buffered. Addressable in 4K byte increments. If the system has a front panel, the board will allow itself to be protected. If there is no front panel, the board will not allow itself to be protected. The board has Bank Address capability, Phantom Disable, MWRITE, and selectable wait states. Bare board $30, board with parts $665. Part No. MEM2



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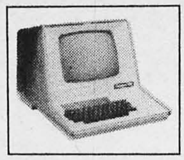
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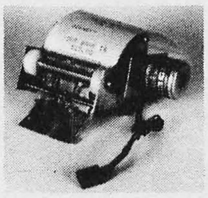
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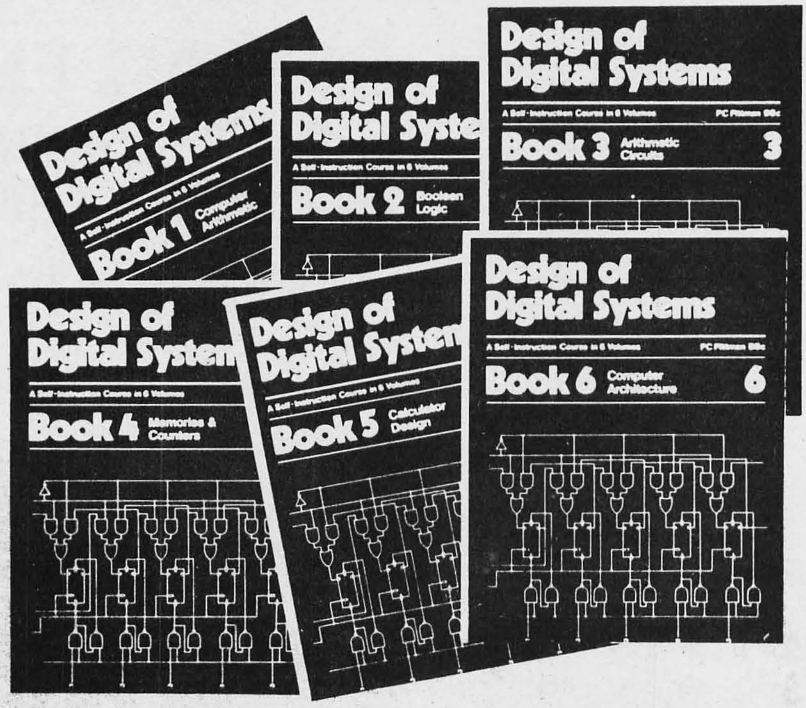
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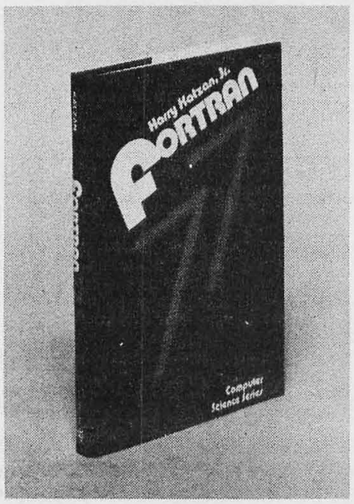
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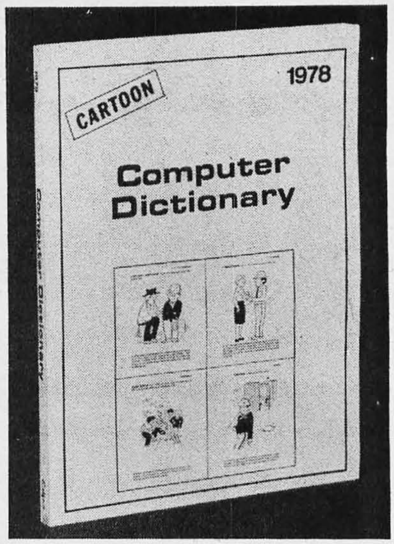
Language characteristics such as statement structure and program organization are discussed. Data types and constants are also described. Coverage of data structures encompasses variables, character string processing, and arrays. Information on the structure of expressions ranges from conventional FORTRAN arithmetic to relational, logical and the new character expressions. The book explains how FORTRAN statements are executed, storage management, the new specification statements in *FORTRAN 77*, the new character assignment, variations inherent in the new control statements, and the new block IF facility for structuring programming.

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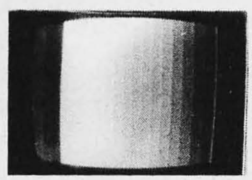
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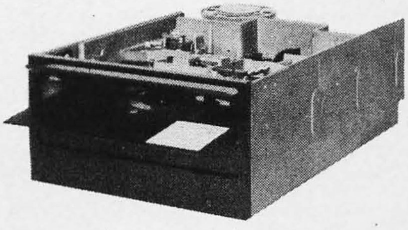
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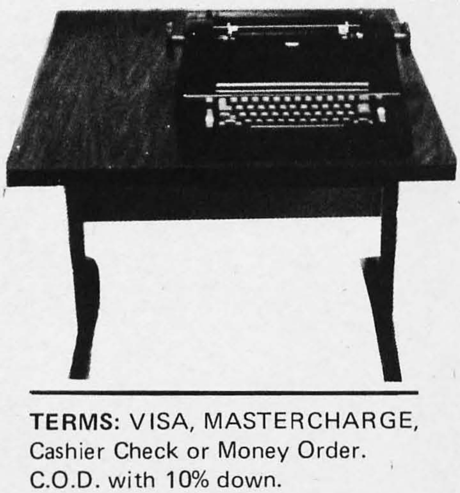
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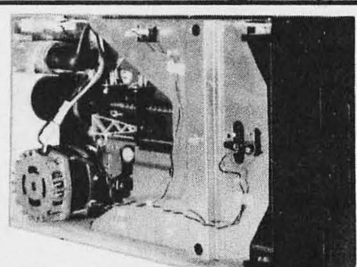
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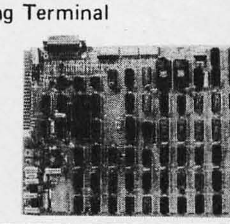
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Scanner and Bulletin Board Tie for First Place BOMB

Two articles tied for first place in the November 1978 BOMB: "Hobbyist Computerized Bulletin Board," by Ward Christensen and Randy Suess (page 150), and "I've Got You in My Scanner! A Computer Controlled Stepper Motor Light Scanner," by Steve Ciarcia (page 76). In second place was "The Sky's the Limit" by Joe Kasser (page 48). The first and second prizes are $100 and $50, respectively.

The third place article was "A Multiuser Data Network" by Robert Bruninga (page 120); fourth place was held by "Functional Approximations" by Fred Ruckdeschel (page 34).■

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The C3 Series is the microcomputer family with the hardware features, high level software and application programs that serious users in business and industry demand from a computer system, no matter what its size.

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Ohio Scientific has developed a remarkable new Information Management system which provides end user intelligence far beyond what you would expect from even the most powerful mini-systems. Basically, it allows end users to store any collection of information under a Data Base Manager and then instantly obtain information, lists, reports, statistical analysis and even answers to conventional "English" questions pertinent to information in the Data Base. OS-DMS allows many applications to be computerized without any programming!

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Ohio Scientific now offers the 6502C microprocessor with 150 nanosecond main memory as the GT option on all C3 Series products. This system performs a memory to register ADD in 600 nanoseconds and a JUMP (65K byte range) in 900 nanoseconds. The system performs an average of 1.5 million instructions per second executing typical end user applications software (and that's a mix of 8, 16 and 24 bit instructions!).

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C3 systems offer the greatest expansion capability in the microcomputer industry, including a full line of over 40 expansion accessories. The maximum configuration is 768K bytes RAM, four 80 million byte Winchester hard disks, 16 communications ports, real time clock, line printer, word processing printer and numerous control interfaces.

Prices you have to take seriously.

The C3 systems have phenomenal performance-to-cost ratios. The C3-S1 with 32K static RAM, dual 8" floppies, RS-232 port, BASIC and DOS has a suggested retail price of under $3600. 80 megabyte disk based systems start at under $12,000. Our OS-CP/M software package with BASIC, FORTRAN and COBOL is only $600. The OS-DMS nucleus package has a suggested retail price of only $300, and other options are comparably priced.

To get the full story on the C3 systems and what they can do for you, contact your local Ohio Scientific dealer or call the factory at (216) 562-3101.

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C3-B wins Award of Merit at WESCON '78 as the outstanding microcomputer application for Small Business.

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